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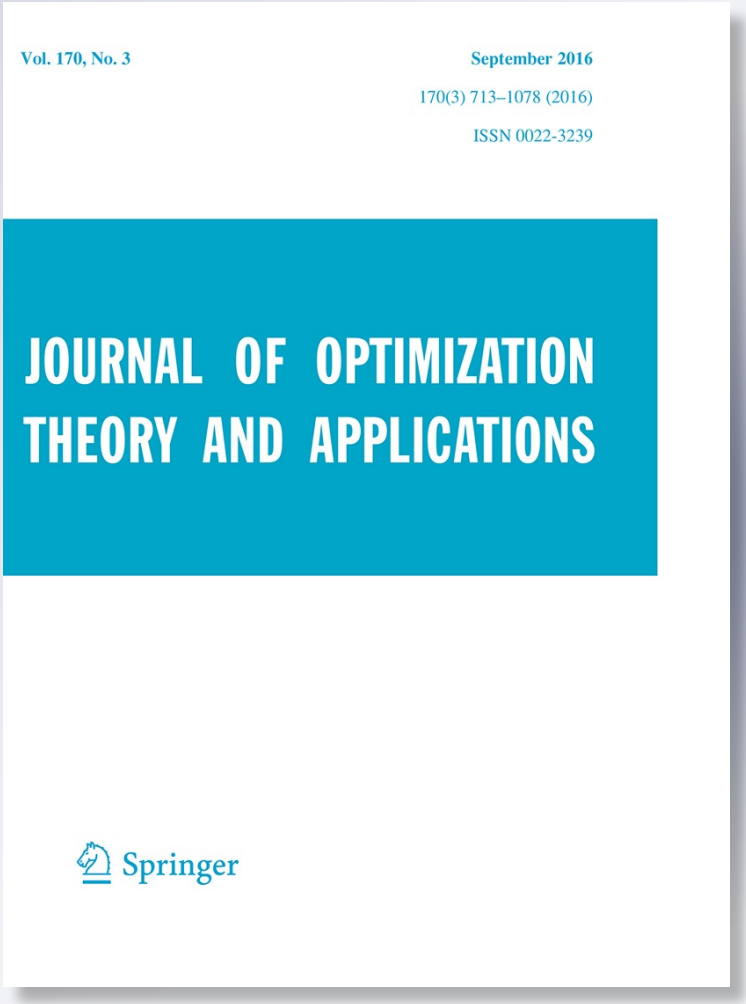

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Optimal VLSI Delay Tuning by Wire Shielding

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Abstract Interconnect shielding is used in VLSI designs to avoid noise interference from the cross-coupling capacitance between adjacent signals. This paper takes advantage of the shields already present in the design and uses them to tune the propagation delay of the clock signals, thus eliminating expensive dedicated delay buffers. The problem of obtaining the desired delay at a minimum shielding cost (silicon area) is formulated as a calculus of variations problem. An analytical solution shows that a square root shield profile is optimal.

Keywords Calculus of variations · Wire shielding · Delay tuning

Mathematics Subject Classification 49K05

1 Introduction

Interconnect shielding is used in very large scale integration (VLSI) designs to avoid noise interference between signals. Shielding wires connected to the supply voltage, that extend adjacently to signal wires avoid the signal switching, that induces noise via *cross-coupling* capacitance to other adjacent signals. In particular, clock signals, which are the noisiest signals and spread over the entire silicon die, are shielded to

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avoid *signal integrity* problems [1]. To ensure the proper synchronization of digital systems, clocks are delayed with respect to each other, which requires the insertion of *delay buffers*. The internal delay of the buffers is subject to unpredictable changes, which has been aggravated by recent progress in VLSI technologies to the nanometer scale [2]. Inserting delay buffers into a clock network is also a delicate task and a design burden.

In this work, we suggest replacing the delay buffers with shields. Shields are already present for clocks, so this replacement does not require extra hardware resources. Delay tuning by wire shields has several advantages over delay buffers. First, wires are considerably less sensitive to manufacturing process variations than delay buffers. This makes the design more robust and its operation in real silicon more predictable [3]. The second advantage is the ease of late design changes, which may cause delays in project schedules. The final but crucial advantage is the elimination of delay buffers, which saves considerable power consumption.

2 Interconnect and Shielding Delays

The *Elmore delay model* is widely used in VLSI designs [4]. Consider Fig. 1a where a *driver* connected on the left side, called the *near-end*, sends a signal along a wire to a *receiver* connected on the opposite side, called the *far-end*. The driver's resistance R_{D} characterizes its driving strength. The receiver has an input capacitance C_{L}, called its *load*.

The interconnection in Fig. 1a has distributed resistance and capacitance, and is usually modeled and approximated by the *RC-ladder* shown in Fig. 1b, where $R_1 = R_{\mathrm{D}}$ and $C_n = C_{\mathrm{L}}$. The driver-to-receiver delay δ is given by [5]

$$\delta \approx \sum_{i=1}^{n} R_i \sum_{j=i}^{n} C_j = \sum_{j=1}^{n} C_j \sum_{i=1}^{j} R_i. \tag{1}$$

VLSI interconnections are designed to meet some predefined delay constraints dictated by the frequency with which the clocks synchronize the operation of the entire

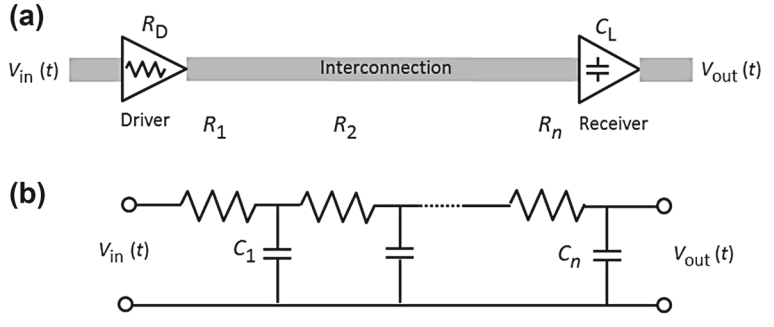

Fig. 1 Driver-to-receiver interconnect (**a**) and its *RC*-ladder modeling (**b**)

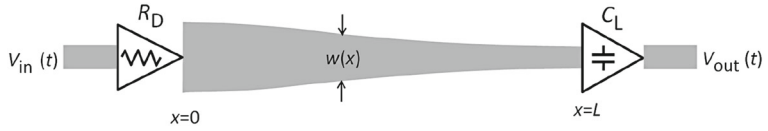

Fig. 2 Tapered interconnect

system. In another setting, the minimization of the delay in (1) is required. To this end, the expression $\sum_{i=1}^{n} R_i \sum_{j=i}^{n} C_j$ shows that a unit length of the wire close to the driver needs to have a small resistance (a wide wire), since it multiplies a large $\sum_{j=i}^{n} C_j$ downstream capacitance. Similarly, the expression $\sum_{j=1}^{n} C_j \sum_{i=1}^{j} R_i$ shows that a unit length of the wire close to the receiver should have small capacitance (a narrow wire) since it multiplies a large $\sum_{i=1}^{j} R_i$ upstream resistance. Consequently, to minimize the propagation delay, the wire should be *tapered*, a topic that has been studied extensively in the literature [6–11]. Figure 2 illustrates a more general interconnection, where the wire width $w(x)$ varies along its traversal $0 \le x \le L$ from the driver to the receiver.

The problem of finding $w(x)$, $0 \le x \le L$, that minimizes (1) was solved in [6]. The authors applied a calculus of variation [12] formulation to the problem. Though VLSI technologies allow only isothetic rectangular shapes, the continuous formulation in [6] highlights very well the nature of the optimal solution. Practically, allowable rectangular shapes can approximate the continuous $w(x)$.

Let $w_{\min}$ be the minimum wire width allowable by the technology in use, and let the resistance and capacitance per $w_{\min} \times w_{\min}$ square of the interconnect metal be r_s and c_s, respectively. The width of the wire $w(x)$ and its length L are expressed as multiplications of $w_{\min}$. By taking $n \to \infty$ in (1), the driver-to-receiver delay is given by

$$\delta = R_D \underbrace{\left(\int_0^L c_s w(x)\,dx + C_L \right)}_{(a)} + \int_0^L \frac{r_s}{w(x)} \underbrace{\left(\int_x^L c_s w(y)\,dy + C_L \right)}_{(b)} dx. \qquad (2)$$

Term (a) in (2) is the downstream capacitance, which is charged though the driver's resistance R_D. Term (b) is the downstream capacitance charged through the resistance $r_s/w(x)$. Fishburn and Schevon found in [6] using the calculus of variations that $w(x)$ minimizing (2) decreases exponentially, as given by the following expression

$$w(x) = \frac{2C_L}{c_s L} W\left(\frac{L}{2} \sqrt{\frac{r_s}{R_D} \frac{c_s}{C_L}} \right) e^{2W\left(\frac{L}{2} \sqrt{\frac{r_s}{R_D} \frac{c_s}{C_L}} \right) \frac{L-x}{L}}, \qquad (3)$$

where W is the Lambert function satisfying $W(x)\, e^{W(x)} = x$.

Interconnecting wires are a source of switching noise, that arises when they toggle between low and high voltage levels; these are termed V_{GND} (usually 0 Volt) and V_{DD} (about 0.8 Volts), respectively. Signals that are a source of significant noise are

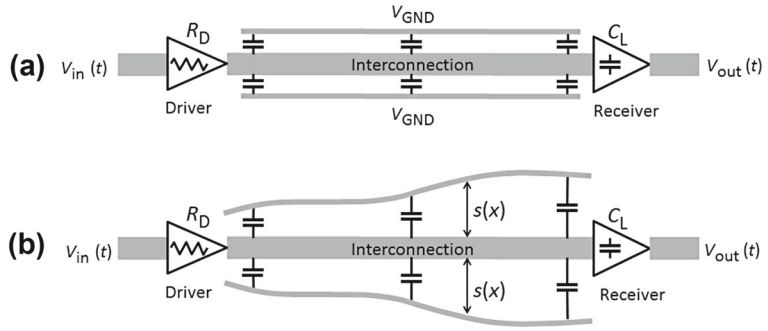

Fig. 3 Shielded interconnect modeling

shielded, where the shielding wires are connected to V_{GND} or V_{DD} [1], as shown in Fig. 3a.

The cross-coupling capacitance between the shielding wires and the interconnect signal introduces further driver-to-receiver propagation delays. This was studied in [13,14], which assumed shielding of fixed spacing from the signal wire, as shown in Fig. 3a, whereas an optimal per-signal delay tuning may require variable spacing, as shown in Fig. 3b. The work in [15] allowed variable spacing. Inspired by the exponential signal interconnect tapering in (3), this solution was assumed to be optimal. As shown below, this assumption is erroneous. Figure 3b depicts a wire of constant width w connecting the driver and the receiver. A two-sided shield extends along the wire, spaced at $s(x)$, $0 \le x \le L$. To make the illustration independent of nanometers and microns, the line-to-line spacing function $s(x)$ is expressed as a multiplication factor of $s_{\min}$, which is the minimum line-to-line spacing allowable. The unit-length line-to-line capacitance of two wires is given by $c_{ll}/s(x)$, where c_{ll} is a technology parameter. It follows from (2) that for a constant width w, the signal wire delay component is

$$\delta_{\text{wire}} = R_D(c_s w L + C_L) + \frac{r_s L}{w}\left(\frac{c_s w}{2} L + C_L\right) \tag{4}$$

When the shield is positioned in a fixed spacing σ, the driver-to-receiver delay component incurred by the shield is

$$\delta_{\text{shield}} = R_D \frac{c_{ll}}{\sigma} L + \frac{r_s c_{ll}}{2\sigma w} L^2 = \frac{c_{ll}}{\sigma} L \left(R_D + \frac{r_s L}{2w}\right). \tag{5}$$

3 Delay Tuning by Continuous Shield Tapering

The driver-to-receiver delay in Fig. 3b $\delta_{\text{wire}} + \delta_{\text{shield}}$ is the sum of two components resulting from the wire and the shield, respectively. Whereas δ_{wire} is known upfront, and thus is not dealt with in the optimization below, δ_{shield} is tuned according to the circumstances caused by the underlying circuits. Let us assume that the space $s(x)$, $0 \le x \le L$ can vary continuously in the range of $0 \le x \le L$, as illustrated in Fig. 3b. It is also assumed that the boundary spacing $s(0) = s_0 > 0$ and $s(L) = s_L > 0$ at the

near-end and at the far-end, respectively, are not predetermined. The driver-to-receiver delay component δ_{shield} is

$$\delta_{\text{shield}} = \underbrace{R_{\text{D}} \int_0^L \frac{c_{\text{ll}}}{s\,(x)} \mathrm{d}x}_{(a)} + \underbrace{\int_0^L \frac{r_{\text{s}}}{w} \left(\int_x^L \frac{c_{\text{ll}}}{s\,(y)} \mathrm{d}y \right) \mathrm{d}x}_{(b)}, \tag{6}$$

whereas the driver-to-receiver delay component δ_{wire} is given by (4). Term (a) in (6) is the delay that occurs when the driver's resistance charges the shield's line-to-line capacitance. Term (b) is the delay associated with the distributed resistance of the interconnecting wire. By rearranging (6), the delay expression caused by shielding is

$$\delta_{\text{shield}} = \int_0^L \left(R_{\text{D}} c_{\text{ll}} \frac{1}{s\,(x)} + \frac{r_{\text{s}} c_{\text{ll}}}{w} \int_x^L \frac{1}{s\,(y)} \mathrm{d}y \right) \mathrm{d}x. \tag{7}$$

Here, we want to obtain a predefined required delay δ_{req}; namely $\delta_{\text{shield}} = \delta_{\text{req}}$. Integrating (7) by parts, where $u = \int_x^L [1/s\,(y)]\,\mathrm{d}y$ and $\mathrm{d}v = \mathrm{d}x$, turns it into

$$\delta_{\text{shield}} = \int_0^L \frac{R_{\text{D}} c_{ll} + (r_s c_{ll}/w)\, x}{s\,(x)} \mathrm{d}x \tag{8}$$

Additionally, the area A between the signal wire and the shielding wire is given by

$$A = \int_0^L s\,(x)\,\mathrm{d}x, \tag{9}$$

and should be minimized. Let us define $F\left(x, s, s'\right) = s\,(x)$, $\phi\left(x, s, s'\right) = [R_{\text{D}} c_{\text{ll}} + (r_{\text{s}} c_{\text{ll}}/w)\, x]/s\,(x)$ and a functional

$$J\,[s\,(x)] = \int_0^L \left[F\left(x, s, s'\right) + \lambda \phi\left(x, s, s'\right) \right] \mathrm{d}x. \tag{10}$$

It is well known in the calculus of variations that by choosing the constant λ appropriately, the extremal of the functional $J\,[s\,(x)]$ in (10) satisfies the following Euler–Lagrange equation [12]

$$\frac{\partial}{\partial s}\left(F + \lambda\phi\right) - \frac{\mathrm{d}}{\mathrm{d}x}\left[\frac{\partial}{\partial s'}\left(F + \lambda\phi\right) \right] = 0,$$

which application for (10) yields

$$1-\lambda\frac{R_{\mathrm{D}}c_{\mathrm{ll}}+\left(r_{\mathrm{s}}c_{\mathrm{ll}}/w\right)x}{s^{2}\left(x\right)}=0. \tag{11}$$

The solution of (11) is

$$s\left(x\right)=\pm\sqrt{\lambda\left(R_{\mathrm{D}}c_{\mathrm{ll}}+\frac{r_{\mathrm{s}}c_{\mathrm{ll}}}{w}x\right)}, \tag{12}$$

where physical considerations imply that the positive root is taken. To verify that the stationary solution in (12) is a minimum, the second derivative of $F+\lambda\phi$ by s is considered, yielding

$$\frac{\partial^{2}\left(F+\lambda\phi\right)}{\partial^{2}s}=\frac{2\lambda\left(R_{\mathrm{D}}c_{\mathrm{ll}}+\frac{r_{\mathrm{s}}c_{\mathrm{ll}}}{w}x\right)}{s^{3}}=\frac{2s^{2}}{s^{3}}=\frac{2}{s}\geq 0. \tag{13}$$

Since $\delta_{\mathrm{shield}}=\delta_{\mathrm{req}}$ is positive and s is continuous and differentiable, $s\left(x\right)<\infty$, $0\leq x\leq L$, strict inequality in (13) holds.

The constant λ still requires determination. By substitution of the boundary spacing $s\left(0\right)\triangleq s_{0}$ in (12), we get

$$\lambda=\frac{s_{0}^{2}}{R_{\mathrm{D}}c_{\mathrm{ll}}}. \tag{14}$$

The final expression of the optimal shield shape is therefore

$$s^{\mathrm{opt}}\left(x\right)=s_{0}\sqrt{1+\frac{r_{\mathrm{s}}}{R_{\mathrm{D}}w}x}. \tag{15}$$

To obtain s_0 the required delay constraint is used. Substitution of (15) in (8) yields

$$\delta_{\mathrm{shield}}=\int_{0}^{L}\frac{R_{\mathrm{D}}c_{\mathrm{ll}}+\left(r_{\mathrm{s}}c_{\mathrm{ll}}/w\right)x}{s_{0}\sqrt{1+\left(r_{\mathrm{s}}/R_{\mathrm{D}}w\right)x}}\mathrm{d}x=\frac{2R_{\mathrm{D}}^{2}c_{\mathrm{ll}}w}{3s_{0}r_{\mathrm{s}}}\left[\left(1+\frac{r_{\mathrm{s}}L}{R_{\mathrm{D}}w}\right)^{\frac{3}{2}}-1\right]=\delta_{\mathrm{req}}, \tag{16}$$

implying

$$s_{0}^{\mathrm{opt}}=\frac{2R_{\mathrm{D}}^{2}c_{\mathrm{ll}}w}{3\delta_{\mathrm{req}}r_{\mathrm{s}}}\left[\left(1+\frac{r_{\mathrm{s}}L}{R_{\mathrm{D}}w}\right)^{\frac{3}{2}}-1\right]. \tag{17}$$

The minimum area is computed as follows:

$$A_{\mathrm{min}}=\int_{0}^{L}s\left(x\right)\mathrm{d}x=\int_{0}^{L}\left(s_{0}^{\mathrm{opt}}\sqrt{1+\frac{r_{\mathrm{s}}}{R_{\mathrm{D}}w}x}\right)\mathrm{d}x=\frac{4R_{\mathrm{D}}^{3}c_{\mathrm{ll}}w^{2}}{9\delta_{\mathrm{req}}r_{\mathrm{s}}^{2}}\left[\left(1+\frac{r_{\mathrm{s}}L}{R_{\mathrm{D}}w}\right)^{\frac{3}{2}}-1\right]^{2}. \tag{18}$$

It is important to note that A_{min} in the left-hand side of (18) is the objective to be minimized, whereas the constraint δ_{req} appears in the denominator of its right-hand

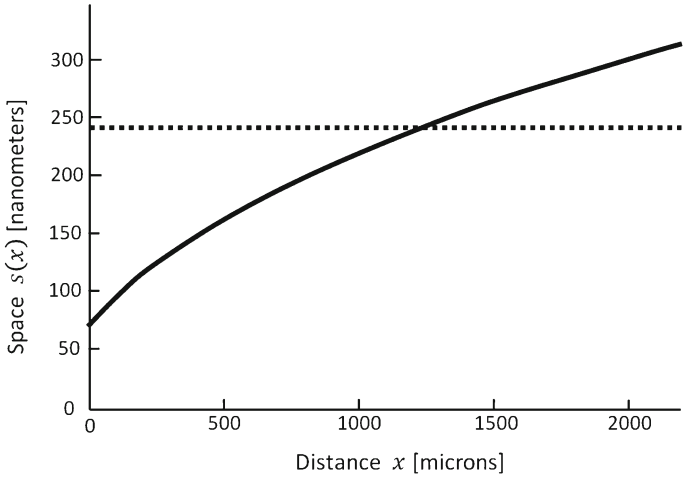

Fig. 4 Optimal shielding compared to shield of constant spacing

side. All the rest terms are problem's parameters. The reciprocal relation between $A_{\min}$ and δ_{req} is indeed what is expected from VLSI circuit considerations.

Given δ_{req}, Fig. 4 illustrates in bold line the shielding shape obtained by (15), yielding minimum area between the signal wire and the shielding wire. We considered a wire of length $L = 2200$ microns and width $w = 0.12$ microns. The driver's resistance R_{D}, the wire's resistance per square r_{s} (called sheet resistance) and the line-to-line capacitance c_{ll} were taken from 65-nanometer VLSI technology. The near-end optimal spacing was calculated by (17) to $s_0 = 0.071$ microns. The dotted line corresponds to a shield with $s\,(x) = \text{const} = 0.24$ microns, which was set to yield the same required delay δ_{req}. The optimal shielding consumes 11 % less area compared to constant spacing.

4 Conclusions

This paper took advantage of the shields already present in VLSI designs, and used them to tune the propagation delay of the clock signals, thus eliminating expensive dedicated delay buffers. The problem of obtaining a desired delay at a minimum shielding cost was formulated as a calculus of variations problem. An analytical solution showed that a square root shield profile is optimal.

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References

1. Salman, E., Friedman, E.G.: High Performance Integrated Circuit Design. McGraw Hill Professional, New York (2012)

2. Agarwal, A., Blaauw, D., Zolotov, V.: Statistical timing analysis for intra-die process variations with spatial correlations. In: Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design, pp. 900–907 (2003)
3. Alioto, M., Palumbo, G., Pennisi, M.: Understanding the effect of process variations on the delay of static and domino logic. IEEE Trans. VLSI Syst. **18**(5), 697–710 (2010)
4. Bakoglu, H.B., Meindl, J.D.: Optimal interconnection circuits for VLSI. IEEE Trans. Electron Devices. **32**(5), 903–909 (1985)
5. Rubinstein, J., Penfield, P.J., Horowitz, M.: Signal delay in RC tree networks. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **2**(3), 202–211 (1983)
6. Fishburn, J.P., Schevron, C.A.: Shaping a distributed-RC line to minimize Elmore delay. IEEE Trans. Circuits Sys. I. **42**(12), 1020–1022 (1995)
7. Fishburn, J.P.: Shaping a VLSI wire to minimize Elmore delay. In: Proceedings of the 1997 European Conference on Design and Test, pp. 244–251 (1997)
8. Chen, C.-P., Wong, D.F.: Optimal wire-sizing function with fringing capacitance consideration. In: Proceedings of the 34th Annual Design Automation Conference (1997)
9. Gao, Y., Wong, D.F.: Wire-sizing optimization with inductance consideration using transmission-line model. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **18**(12), 1759–1767 (1999)
10. Zhang, H., Wong, M.D., Chao, K.-Y., Deng, L.: Wire shaping is practical. In: Proceedings of the 2009 International Symposium on Physical Design, pp. 131–138 (2009)
11. El-Moursy, M.A., Friedman, E.G.: Wire shaping of RLC interconnects. Integr. VLSI J. **40**(4), 461–472 (2007)
12. Fox, C.: An Introduction to the Calculus of Variations. Dover, New York (1987)
13. Kahng, A.B., Muddu, S., Sarto, E.: Tuning strategies for global interconnects in high-performance deep-submicron ICs. VLSI Des. **10**(1), 21–34 (1999)
14. Jakushokas, R., Friedman, E.G.: Resource based optimization for simultaneous shield and repeater insertion. IEEE Trans. VLSI Syst. **18**(5), 742–749 (2010)
15. Karami, M.A., Afzali-Kusha, A.: Exponentially tapering ground wires for Elmore delay reduction in on chip interconnects. In: Proceedings of the 2006 International Conference on Microelectronics, pp. 99–102 (2006)