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On optimal ordering of signals in parallel wire bundles

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Abstract

Optimal ordering and sizing of wires in a constrained-width interconnect bundle are studied in this paper. It is shown that among all possible orderings of signal wires, a monotonic order of the signals according to their effective driver resistance yields the smallest weighted average delay. Minimizing weighted average delay is a good approximation for MinMax delay optimization. Three variants of monotonic ordering are proven to be optimal, depending on the Miller coupling factors (*MCF*) ratio between the signals at the sides of the bundle and that of the internal wires. The monotonic order property holds for a very broad range of VLSI circuit settings arising in common design practice. A simple, yet near-optimal, setting of wire widths within the bundle to yield the best average weighted delay is proposed. The theoretical results have been validated by numerical experiments on 65 nm process technology and industrial design data. In all cases the ordering optimization yielded improvement in the range of 10% in wire delay, translated to about 5% improvement in the clock cycle of a high-performance microprocessor implemented in that technology.

Keywords: Routing; Wire ordering; Wire spacing

1. Introduction

Cross capacitances between wires in interconnect structures have a major effect on circuit timing. The importance of this effect grows with technology scaling [1,2]. In this paper, delays in a bundle of parallel wires with different drivers and loads are minimized by choosing an optimal ordering of the nets. A model for the bundle of wires is shown in Fig. 1(a). It represents a common CMOS layout configuration, where interconnect wires run in parallel between two power supply or shielding rails, such that the total width of the structure A is a fixed constraint. An abstraction of actual layout is made by assuming that all drivers and all receivers are located at the ends of the structure of length L. Real layouts can be decomposed into several such structures using effective drivers and receivers, since long segments of parallel wires are very common in industrial practice, mostly when high metal layers are concerned. The wire delays in the model of Fig. 1(a) are typically dominated by cross capacitances between adjacent wires, since the ratio between wire thickness and wire width tends to grow with non-uniform technology scaling [3]. Therefore, delays can be optimized by allocation of inter-wire spaces. In addition, wire widths can be set to optimize wire resistances. Furthermore, reordering of the wires can improve the timing, because critical wires can be put next to each other and share the largest spaces, which have the smallest cross capacitances.

Reordering of the bundle wires is a new degree of freedom in timing optimization, which has not been explored in the past. The main result of this paper is that the signal ordering is highly beneficial and can typically be solved independently of the wire sizing. Moreover, the optimal order can be derived directly from the parameter setting of the given problem, by positioning the wires according to the effective resistances of their drivers.

Wire order within the bundle yielding minimal delays must be monotonic in the strength of the driver. The type of the monotonic order depends on Miller coupling factors (*MCF*) occurring at the side signals of the bundle.

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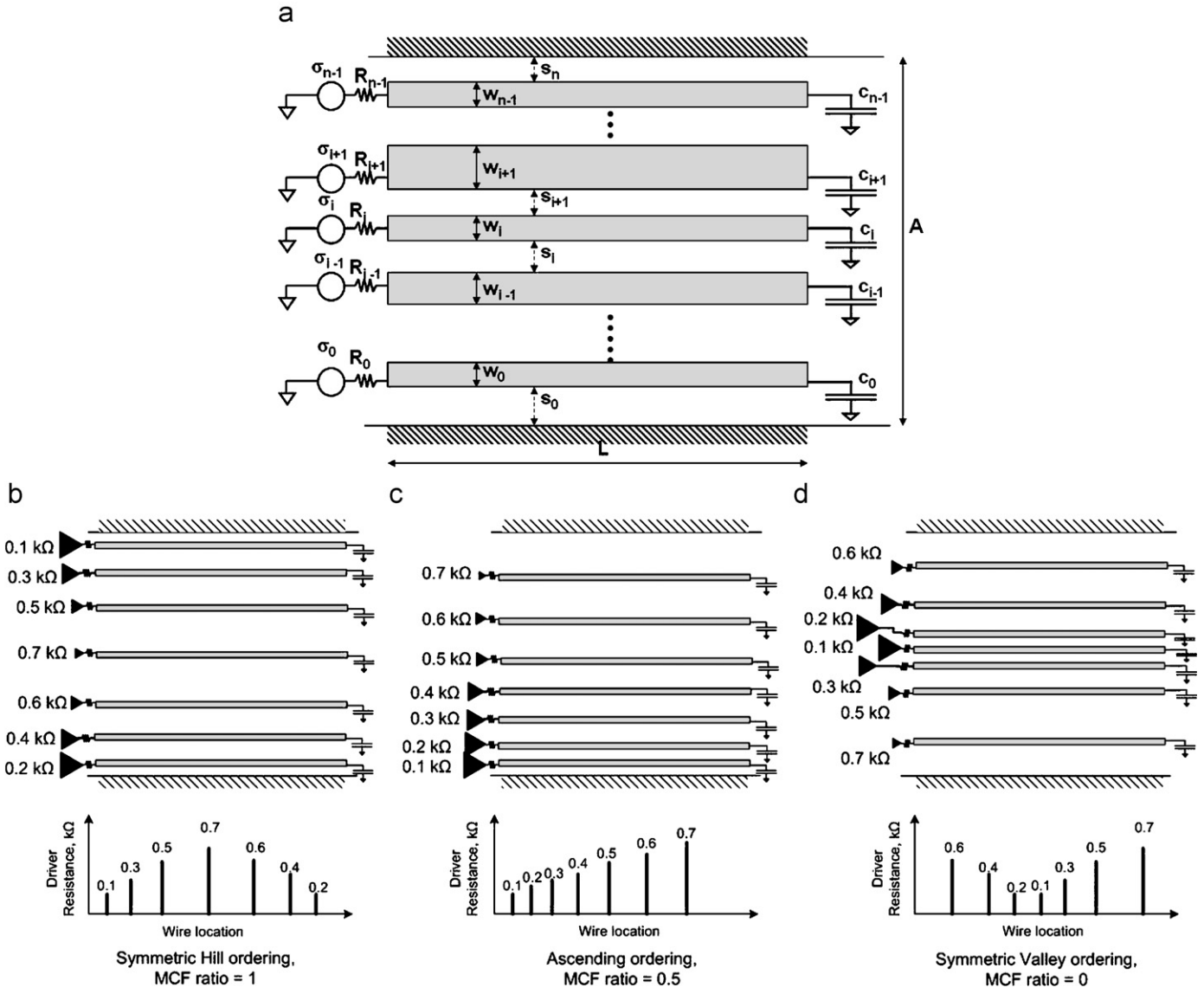

Fig. 1. (a) Signal drivers (modeled as voltage sources with series resistances), interconnect bundle wires of length L, and receivers (modeled as load capacitances). Timing optimization is performed by reordering the signal wires and by allocating wire widths and spaces, for a given constrained channel width A. (b–d) present the optimal order of signals and the corresponding wire-to-wire space allocation for various ratios of *MCF* between extreme and internal signals.

Only three types of monotonic order can yield the minimal delay, regardless of the specific driver strengths. These are illustrated in Figs. 1(b–d). Fig. 1(b) illustrates the case of uniform *MCF* (e.g. when the sidewalls of the bundle are not power supplies but rather arbitrary logical signals); the corresponding optimal order is called "symmetric hill", where the signals with the weakest drivers are located at the center of the bundle, and their corresponding spaces are the largest. Fig. 1(c) illustrates the case where *MCF* at the sidewalls is half of the *MCF* between internal wires in the bundle (e.g. when sidewalls are connected to power supplies such that their *MCF* is 1, while internal *MCF* of 2 is assumed). The corresponding optimal order is ascending, where the weakest driver resides on one side of the bundle and the strongest driver resides at the other side. Fig. 1(d) corresponds to a case where the *MCF* at the sidewall is assumed to be zero (e.g. when active shielding [4] is employed at the sidewalls), corresponding to a "symmetric valley".

Net ordering for delay optimization has not been addressed in previous works. For a fixed order of wires, the problem of allocating widths and spaces to maximize performance in tuning of bus structures was proposed in [5] and solved in [6]. The wire-sizing problem has been addressed in [7,8] for a single net. Sizing and spacing multiple nets with consideration of coupling capacitance have been addressed in [9] for general interconnect layouts by converting cross capacitance to effective fringe capacitance. Coupling capacitance has been addressed explicitly in the context of physical design for

minimizing crosstalk noise [10,11] or dynamic power [12]. Some authors treated wire sizing for throughput optimization in buses using uniform wire widths and spaces [13–15]. Several variants of net reordering have been applied for improving layout efficiency [16], and for noise reduction [11,17–20]. Swapping of wires for power reduction was applied in [21]. Vittal et al. [17] suggested without proof to reduce crosstalk noise by sorting wires in order of driver strength, which is closely related to our result in delay minimization.

2. Problem formulation

Consider a bundle of n signal nets $\sigma_0,\ldots,\sigma_{n-1}$ between two sidewalls (wires at fixed locations) as shown in Fig. 1. S_i and S_{i+1}, respectively, denote spaces to neighbors of wire W_i. The length of each wire is L. Each wire is driven by a driver with output resistance R_i and loaded by receiver with capacitance C_i. The sum of wire widths and spaces between the sidewalls is given in the following constraint (2.1), which represents the total width A of the available area for laying out the bundle of wires.

$$g(\bar{W},\bar{S}) = \sum_{j=0}^{n-1} W_i + \sum_{j=0}^{n} S_i = A. \tag{2.1}$$

Signal delays are expressed by an Elmore model using simple approximations for wire capacitances and wire resistance. The delay of signal σ_i is given in [6] by

$$\Delta_i(\bar{W},\bar{S}) = a + R_i(kW_i + g + C_i) + \frac{b + eC_i}{W_i} + \left(hR_i + \frac{d}{W_i}\right)\left(\frac{1}{S_i} + \frac{1}{S_{i+1}}\right). \tag{2.2}$$

The coefficients a, b, d, e, k, g, h are technology dependent parameters. This model includes effects of wire resistance (inversely proportional to wire width W_i) and effects of wire capacitance terms (area capacitance is proportional to W_i, cross capacitances to neighboring wires are inversely proportional to spaces S_i and S_{i+1}). Note that only nearest-neighbor wires are included, because the adjacent upper and lower metal layers are assumed to be dense, and serve as effective shields for capacitive coupling to other wires in the bundle. Although the Elmore model is a first-order approximation and it does not account for input waveform slope [22], it is widely applicable in interconnect optimization due to its high-fidelity property [23]. The absolute accuracy of the model can also be improved, by using parameter fitting as described in [24]. The model is used in this work because of its simplicity in mathematical analysis, while the delay improvements are verified by SPICE simulations. MCF can be included in the last term to account for crosstalk effect on delay uncertainty [25]. Typically, $MCF = 2$ is assumed when neighbor wires switch in the opposite direction causing increased delays, while $MCF = 0$ is assumed for same-direction switching and reduced delay. We assume first that $MCF = 1$ for all of the signals, yielding nominal delay values.

Let $\pi \in \Pi$ denote an ordering (permutation) of the signals in the interconnect bundle, taken from the set of all $n!$ possible orders. We are seeking an ordering π^* of the bundle signals, which after wire width and space allocation yields the minimum objective function representing some delay characteristic. In practice, the useful delay objective function is the maximal worst slack among all signals and the optimization attempts to minimize this maximum

$$f_1(\pi,\bar{W},\bar{S}) = \max_{0\leqslant i\leqslant n-1}\{\Delta_i(\bar{W},\bar{S}) - T_i\}, \tag{2.3}$$

where T_i is required arrival time of the ith signal. Note that we exchanged the terms of the slack for the sake of mathematical convenience. This design scenario calls for MinMax optimization problems. Such problems are hard to solve analytically since they are not differentiable. Maximization of average wire slack, which is equivalent to minimization of average delay or minimization of the total sum of delays, is given as

$$\begin{aligned} f_2(\pi,\bar{W},\bar{S}) &= \sum_{i=0}^{n-1}\Delta_i(\pi,\bar{W},\bar{S}) \\ &= \sum_{i=0}^{n-1}\Big\{a + R_i(kW_i + g + C_i) \\ &\quad + \frac{b + eC_i}{W_i} + \left(hR_i + \frac{d}{W_i}\right)\left(\frac{1}{S_i} + \frac{1}{S_{i+1}}\right)\Big\}. \end{aligned} \tag{2.4}$$

This objective function is mathematically convenient because it is differentiable, and it is also a useful performance metric in industrial practice [6].

Minimization of maximal slack (2.3) can be approached by introducing weights in (2.4). We define the following objective:

$$\begin{aligned} f_3(\pi,\bar{W},\bar{S}) &= \sum_{i=0}^{n-1}\alpha_i\Delta_i(\pi,\bar{W},\bar{S}) = \sum_{i=0}^{n-1}\alpha_i\Big\{a + R_i(kW_i + g + C_i) \\ &\quad + \frac{b + eC_i}{W_i} + \left(hR_i + \frac{d}{W_i}\right)\left(\frac{1}{S_i} + \frac{1}{S_{i+1}}\right)\Big\}, \end{aligned} \tag{2.5}$$

where α_i is a normalized estimation of signal criticality. The least critical signal (with maximal T_i) will have $\alpha = 1$, all the others will have values larger than 1. In other words (2.5) represents the *total sum of wire delays weighted by signal criticality*. This objective incorporates good properties of (2.3) and (2.4): on the one hand (2.5) is a differentiable function; on the other hand, weighting delays by signal criticality makes it similar to (2.3), which is more useful in practice than (2.4).

Assume for the moment that the order π of the signals in the bundle is given. For minimizing (2.5) subject to (2.1) we

differentiate f_3 and g by all of their sizing variables:

$$\begin{cases} \frac{\partial f_3}{\partial W_i} = \alpha_i\left(kR_i - \frac{eC_i+b}{W_i^2} - \frac{d}{W_i^2}\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right)\right), \\ \quad 0 \leqslant i \leqslant n-1; \\ \frac{\partial f_3}{\partial S_i} = -\frac{1}{S_i^2}\left[h(\alpha_{i-1}R_{i-1}+\alpha_i R_i) + d\left(\frac{\alpha_{i-1}}{W_{i-1}}+\frac{\alpha_i}{W_i}\right)\right], \\ \quad 0 < i \leqslant n-1; \\ \frac{\partial f_3}{\partial S_0} = -\frac{\alpha_0}{S_0^2}\left[hR_0 + \frac{d}{W_0}\right]; \\ \frac{\partial f_3}{\partial S_n} = -\frac{\alpha_{n-1}}{S_n^2}\left[hR_{n-1} + \frac{d}{W_{n-1}}\right]; \\ \frac{\partial g}{\partial W_i} = 1, \quad 0 \leqslant i \leqslant n-1; \\ \frac{\partial g}{\partial S_i} = 1, \quad 0 \leqslant i \leqslant n. \end{cases} \tag{2.6}$$

At the minimum there exists some real number λ (Lagrange multiplier), satisfying $\nabla f = \lambda \nabla g$. Rearranging and substituting yields the following:

$$\begin{cases} \lambda = \alpha_i\left(kR_i - \frac{eC_i+b}{W_i^2} - \frac{d}{W_i^2}\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right)\right), \\ \qquad 0 \leqslant i \leqslant n-1; \\ \lambda = -\frac{1}{S_i^2}\left[h(\alpha_{i-1}R_{i-1}+\alpha_i R_i) + d\left(\frac{\alpha_{i-1}}{W_{i-1}}+\frac{\alpha_i}{W_i}\right)\right], \\ \qquad 0 < i \leqslant n-1; \\ \lambda = -\frac{\alpha_0}{S_0^2}\left[hR_0 + \frac{d}{W_0}\right]; \\ \lambda = -\frac{\alpha_n}{S_n^2}\left[hR_{n-1} + \frac{d}{W_{n-1}}\right]. \end{cases}$$

The above equations and the area constraint (2.1) impose $2n+2$ algebraic equations in $2n+2$ unknown variables λ, $W_0,\ldots,W_{n-1}$, $S_0,\ldots,S_n$. Solving and substituting into (2.5) produces minimal weighted total sum of signal delays for the assumed order π.

The order of wires affects the sum of delays primarily because every driver pair of adjacent signal is associated with a shared cross capacitance between the wires. It makes sense to allocate large spaces to a wire driven by a weak driver or a wire with high criticality, in order to reduce the driver's load. Strong drivers and non-critical nets can cope with large cross capacitances resulting in narrow spaces. Consequently, in order to best utilize the total area given for the wire bundle, weak drivers or highly critical nets should share the same large space. Similarly, strong drivers or non-critical nets can share a small inter-wire space. The space sharing idea is illustrated in Fig. 2. There, the bundle is comprised of some signals with weak drivers (W) and some with strong drivers (S). For equal criticality, the ordering in Fig. 2(b) is superior to Fig. 2(a), which is apparently the worst. Wire sizing and spacing optimization aiming at minimizing the total sum of delays will yield smaller (better) delays for configuration 2(b), in comparison with 2(a).

Consider now $\pi \in \Pi$ as variable, and find the order for which optimal wire sizing and spacing yields minimum

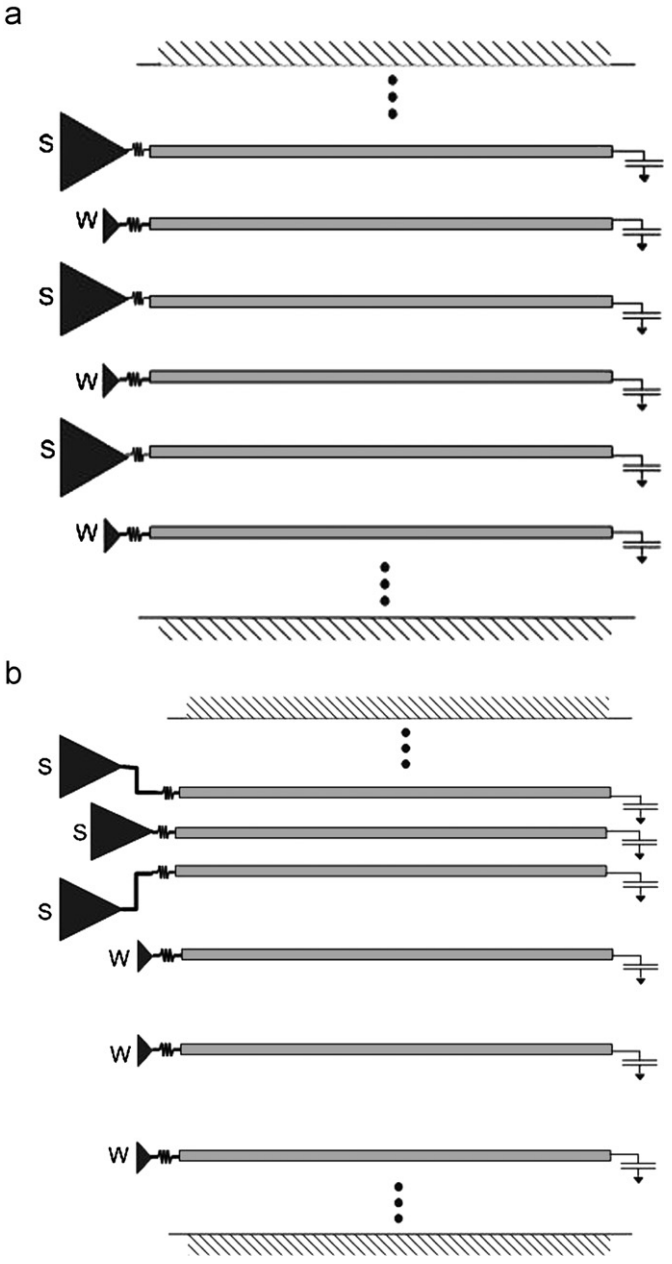

Fig. 2. Space sharing in two interconnects channel configurations. (a) Interleaved placement of strong and weak drivers, (b) sorted placement of signals according to driver strength.

total weighted sum of delays, as discussed in the previous section. One needs therefore to solve the following problem:

$$\begin{cases} \min\limits_{\pi \in \Pi} f_3(\pi, \bar{W}, \bar{S}); \\ \sum\limits_{j=0}^{n-1} W_i + \sum\limits_{j=0}^{n} S_i = A. \end{cases}$$

In this formulation, both signal ordering and wire sizing are considered simultaneously.

3. Optimality of symmetric hill order

3.1. Wires of uniform width

For the sake of clarity, assume first that all the wires have the same width W while spaces can vary among wires. Hence, wire sizing means finding the optimal W and allocating optimal spaces between wires. Assume for the moment that W is uniform and predetermined. For any order $\pi\in\Pi$, minimizing the total sum of delays involves only $n+1$ variables $(S_0,\ldots,S_n)$. The following conditions are necessary for optimum:

$$\frac{\partial f}{\partial S_i}+\lambda\frac{\partial g}{\partial S_i}=0,\quad 0\leqslant i\leqslant n, \tag{3.1}$$

$$\begin{aligned}\frac{\partial f}{\partial S_i}&=-\frac{d(\alpha_{i-1}+\alpha_i)}{WS_i^2}-\frac{h(\alpha_{i-1}R_{i-1}+\alpha_iR_i)}{S_i^2}\\&=0,\quad 0<i<n,\end{aligned} \tag{3.2}$$

$$\begin{cases}\frac{\partial f}{\partial S_0}=-\frac{d\alpha_0}{WS_0^2}-\frac{h\alpha_0R_0}{S_0^2};\\ \frac{\partial f}{\partial S_n}=-\frac{d\alpha_{n-1}}{WS_n^2}-\frac{h\alpha_{n-1}R_{n-1}}{S_n^2};\\ \frac{\partial g}{\partial S_i}=1,\quad 0\leqslant i\leqslant n.\end{cases} \tag{3.3}$$

Substitution of (3.3) and (3.2) into (3.1) yields

$$\begin{cases}\lambda=\frac{1}{S_i^2}\left(\frac{d(\alpha_{i-1}+\alpha_i)}{W}+h(\alpha_{i-1}R_{i-1}+\alpha_iR_i)\right),\quad 0<i<n;\\ \lambda=\frac{1}{S_0^2}\left(\frac{d\alpha_0}{W}+h\alpha_0R_0\right);\\ \lambda=\frac{1}{S_n^2}\left(\frac{d\alpha_{n-1}}{W}+h\alpha_{n-1}R_{n-1}\right).\end{cases} \tag{3.4}$$

From (3.4) we obtain the following expressions for spaces at the optimum:

$$\begin{cases}S_i=\sqrt{\frac{1}{\lambda}\left(\alpha_i\left(\frac{d}{W}+hR_i\right)+\alpha_{i-1}\left(\frac{d}{W}+hR_{i-1}\right)\right)},\\ \qquad\qquad 0<i<n;\\ S_0=\sqrt{\frac{1}{\lambda}\alpha_0\left(\frac{d}{W}+hR_0\right)};\\ S_n=\sqrt{\frac{1}{\lambda}\alpha_{n-1}\left(\frac{d}{W}+hR_{n-1}\right)}\end{cases} \tag{3.5}$$

These optimal spaces depend on resistances of the signal drivers, but are independent of capacitive loads. Substitution of (3.5) into (2.1) yields the following expression for λ

$$\begin{aligned}\lambda=\frac{1}{(A-nW)^2}&\left(\sum_{i=1}^{n-1}\sqrt{\alpha_i\left(\frac{d}{W}+hR_i\right)+\alpha_{i-1}\left(\frac{d}{W}+hR_{i-1}\right)}\right.\\&\left.+\sqrt{\alpha_0\left(\frac{d}{W}+hR_0\right)}+\sqrt{\alpha_{n-1}\left(\frac{d}{W}+hR_{n-1}\right)}\right)^2.\end{aligned} \tag{3.6}$$

Further substitution into (2.5) produces the following expression for the minimal weighted total sum of delays.

$$f_3=f^{\mathrm{I}}+f^{\mathrm{II}}, \tag{3.7}$$

where

$$\begin{aligned}f^{\mathrm{I}}=&n\left(a+\frac{b}{W}\right)\sum_{i=0}^{n-1}\alpha_i+(kW+g)\sum_{i=0}^{n-1}R_i\alpha_i\\&+\frac{e}{W}\sum_{i=0}^{n-1}C_i\alpha_i+\sum_{i=0}^{n-1}R_iC_i\alpha_i\end{aligned}$$

and

$$\begin{aligned}f^{\mathrm{II}}=\frac{1}{A-nW}&\left[\sum_{i=1}^{n-1}\sqrt{\alpha_i\left(\frac{d}{W}+hR_i\right)+\alpha_{i-1}\left(\frac{d}{W}+hR_{i-1}\right)}\right.\\&\left.+\sqrt{\alpha_0\left(\frac{d}{W}+hR_0\right)}+\sqrt{\alpha_{n-1}\left(\frac{d}{W}+hR_{n-1}\right)}\right]^2.\end{aligned}$$

The first term f^{I} is invariant for different orders of signals. In the second term f^{II}, the indices of adjacent signals interact with each other in square root terms, thus making f^{II} dependent on the order of signals in the bundle. The physical reason for this is that cross capacitance between adjacent wires is determined by the space they share with each other. The question of what is the order $\pi\in\Pi$ that minimizes f^{II}, is therefore important. As proven below, symmetric hill ordering, which captures the above reasoning, yields the minimum of average weighted wire delay.

Definition 3.1. *Effective signal resistance*: Let R be the resistance of the driving gate, W be the signal wire width and α be the signal criticality. The term $\Re=\alpha(d/W+hR)$ is called *effective signal resistance*.

Definition 3.2. *Successive roots sum*: Let $(\Re_0,\ldots,\Re_{n-1})$ be sequences of positive real numbers. The term $\sqrt{\Re_0}+\sum_{i=1}^{n-1}\sqrt{\Re_{i-1}+\Re_i}+\sqrt{\Re_{n-1}}$ is called *successive roots sum (SRS)*.

Definition 3.3. *Symmetric hill ordering*: Let $\Re_0\leqslant\Re_1\leqslant,\cdots,\Re_{n-2}\leqslant\Re_{n-1}$ be a sequence of n positive real numbers increasingly ordered. Let us split it into even and odd interleaved subsequences $\Re_0\leqslant\Re_{2,}\cdots$,and $\Re_1\leqslant\Re_3\leqslant,\cdots$, reverse the order of numbers in the even subsequence, thus turning it into monotonic decreasing sequence. Finally, concatenate the even and the modified (reversed) odd subsequences into one sequence. The new sequence thus obtained is said to be ordered in *symmetric hill ordering* (as it resembles climbing and descending a symmetric hill). Fig. 3 illustrates how such order is obtained.

Property 3.1. *Pair swapping*: Let $(\Re_i,\ \Re_{i+1},\ \Re_{i+2},\ldots,\ \Re_{i+k-2},\ \Re_{i+k-1},\ \Re_{i+k})$, $k\geqslant 3$ be a sequence of real positive numbers, such that $\Re_{i+1}\geqslant\Re_{i+k-1}$ (called internal pair) and $\Re_i\leqslant\Re_{i+k}$ (called external pair). Then the inversion of subsequence $(\Re_{i+1},\ \Re_{i+2},\ldots,\Re_{i+k-2},\ \Re_{i+k-1})$ into $(\Re_{i+k-1},\ \Re_{i+k-2},\ldots,\ \Re_{i+2},\ \Re_{i+1})$ decreases the SRS of the sequence.

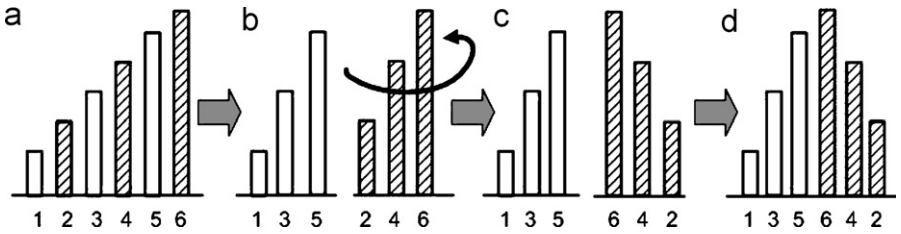

Fig. 3. Construction of symmetric hill ordering: (a) sort numbers in ascending order; (b) split sequence into odd and even subsequences; (c) reverse order of numbers in the even subsequence; (d) concatenate the odd and the modified subsequences.

Proof. Since only neighbors of $\Re_i$, $\Re_{i+1}$, $\Re_{i+k-1}$, $\Re_{i+k}$ are changed, it is sufficient to prove that $\sqrt{\Re_i+\Re_{i+1}}+\sqrt{\Re_{i+k-1}+\Re_{i+k}} \geqslant \sqrt{\Re_i+\Re_{i+k-1}}+\sqrt{\Re_{i+1}+\Re_{i+k}}$. Squaring the two sides one needs to show that $(\Re_i+\Re_{i+1})\times(\Re_{i+k-1}+\Re_{i+k}) \geqslant (\Re_i+\Re_{i+k-1})\times(\Re_{i+1}+\Re_{i+k})$. Expanding both sides, it is left to show that $(\Re_i-\Re_{i+k})\times(\Re_{i+k-1}-\Re_{i+1})\geqslant 0$, which indeed follows from the assumption on the relations of the internal and external pairs. □

Property 3.2. *Optimal insertion of maximal value*: Let $(\Re_0,\ldots,\Re_{n-1})$ be a sequence of positive real numbers ordered as a symmetric hill. Let $\Re > \max\{\Re_0,\ldots,\Re_{n-1}\}$. Then the location where inserting $\Re$ into the sequence minimizes the new SRS, is at the center between the two largest numbers. Hence the new sequence is also in symmetric hill order.

Proof. Let us insert $\Re$ arbitrarily into the sequence between $\Re_i$ and $\Re_{i+1}$, thus resulting in the quadruples $(\Re_{i-1}, \Re_i, \Re, \Re_{i+1})$ and $(\Re_i, \Re, \Re_{i+1}, \Re_{i+2})$ in the new sequence of $n+1$ numbers. If $\Re_i$ and $\Re_{i+1}$ were not the two center numbers of the old sequence (top of the hill), at least one of these quadruples satisfies the condition of *pair swapping* Property 3.1. Therefore, the SRS of the new sequence can be reduced by appropriate swapping of $\Re$ with its left or right neighbor. If $\Re$ is inserted before $\Re_1$ or after $\Re_n$, a direct calculation shows that swapping $\Re$ with $\Re_1$ (or $\Re_n$) decreases the resulting SRS. The only position where the pair swapping Property 3.1 condition does not exist is in between the two largest numbers of the old sequence. Such insertion creates a new sequence satisfying symmetric hill order. □

Definition 3.4. *Local maximum*: Let $(\Re_0,\ldots,\Re_{n-1})$ be a sequence of positive real numbers. The number $\Re_j$, is called a *local maximum* of $(\Re_0,\ldots,\Re_{n-1})$ if both $\Re_j \geqslant \Re_{j-1}$ and $\Re_j \geqslant \Re_{j+1}$.

Property 3.3. *Local maximum elimination*: Let $(\Re_0,\ldots,\Re_{n-1})$ be a sequence of positive real numbers. Let $(\Re_i, \Re_{i+1})$ and $(\Re_j, \Re_{j+1}, \Re_{j+2})$ be two disjoint subsequences, where $\Re_{j+1}$ is a local maximum and $\Re_i \geqslant \Re_{j+1} \geqslant \Re_{i+1}$. Then, repositioning $\Re_{j+1}$ in between $\Re_i$ and $\Re_{i+1}$ decreases the SRS of the sequence.

Proof. We need to show that

$$\sqrt{\Re_i+\Re_{i+1}}+\sqrt{\Re_j+\Re_{j+1}}+\sqrt{\Re_{j+1}+\Re_{j+2}} \geqslant \sqrt{\Re_i+\Re_{j+1}}+\sqrt{\Re_{j+1}+\Re_{i+1}}+\sqrt{\Re_j+\Re_{j+2}}.$$

Let us denote

$$p=\Re_i/\Re_{j+1}\geqslant 1,\quad q=\Re_{i+1}/\Re_{j+1}\leqslant 1,$$
$$r=\Re_j/\Re_{j+1}\leqslant 1,\quad s=\Re_{j+2}/\Re_{j+1}\leqslant 1.$$

Therefore, we need to show that $\sqrt{p+q}+\sqrt{r+1}+\sqrt{1+s}\geqslant\sqrt{p+1}+\sqrt{1+q}+\sqrt{r+s}$. Rearranging, this is equivalent to:

$$\sqrt{r+1}+\sqrt{1+s}-\sqrt{r+s}\geqslant\sqrt{p+1}+\sqrt{1+q}-\sqrt{p+q}. \tag{3.8}$$

Since $r\leqslant 1$, it follows that left-hand side of (3.8) is monotonic decreasing in s, thus minimized for $s=1$. Since $p\geqslant 1$, it follows that right-hand side of (3.8) is monotonic increasing in q, thus maximized for $q=1$. So if the inequality still holds for the minimal value of left-hand side and maximal value of right-hand side, (3.8) does always hold. Indeed, substitution of $s=1$ and $q=1$ we obtain $\sqrt{r+1}+\sqrt{2}-\sqrt{r+1}=\sqrt{2}+\sqrt{1+q}-\sqrt{1+q}$. □

Based on the above properties, we are ready to prove the theorem of optimal signal ordering in a bundle of parallel wires.

Theorem 3.1. *(Optimal ordering of uniform-width wires): Let a signal bundle have arbitrary drivers, arbitrary capacitive loads, arbitrary required arrival times and uniform wire width. Let MCF be the same for all signal pairs, including the sidewalls. Then the symmetric hill ordering of the signals in the bundle according to their effective driver resistance yields minimum total weighted sum of delays.*

Proof. It was shown in (3.7) that for any order of the signals, the minimized total sum of delays f_3 consists of two terms f^{I} and f^{II}. The term f^{I} captures the delays resulting from the capacitive loads, a component that is independent of the signal order in the bundle. The term f^{II} captures the delay contributed by the cross capacitances of the signals, a component which depends on the signal order. It is therefore sufficient to minimize f^{II}.

Let $\pi^*=(\Re_0,\ldots\Re_{n-1})$ be the effective driver resistance symmetric hill ordering of the bundle, and denote by $f^{\mathrm{II}}(\pi^*)$ the corresponding term in the minimized total sum

of delays thus obtained. We'll show by induction that for any other ordering π of effective driver resistances $f^{II}(\pi^*) \leqslant f^{II}(\pi)$.

For a bundle comprised of one or two signals the induction hypothesis trivially exists. For a bundle of three signals, the optimality of symmetric hill ordering follows from the optimal insertion Property 3.2. Put the two smaller effective resistances, say $\Re_a$ and $\Re_b$ in the bundle first. Then, the optimal insertion Property 3.2 dictates the location of $\Re_c$ at the center, thus resulting in symmetric hill order. If $\Re_a$ ($\Re_b$) and $\Re_c$ are placed first, a direct calculation shows that $\Re_b$ ($\Re_a$) needs to reside such that $\Re_c$ is located at the center.

By the induction hypothesis, the symmetric hill order is optimal for any $n-1$ signals bundle. Assume on the contrary that there exists a n signal bundle whose optimal order π' is not symmetric hill. It follows from the non optimality of π^* that $f^{II}(\pi^*) > f^{II}(\pi')$.

Let ($\Re_l$, $\Re_x$, $\Re_r$) be the center triplet of π^*, namely, $\Re_x$ is the largest resistance. There are two possibilities: triplet ($\Re_l$, $\Re_x$, $\Re_r$) exists or does not exist in π'.

If it exists, let us delete $\Re_x$ from both π' and π^*, thus inducing bundles of $n-1$ signals $\pi'^{,n-1}$ and $\pi^{*,n-1}$. The first is not symmetrically hill ordered, while the second is. It follows from the induction hypothesis that $f^{II}(\pi^{*,n-1}) < f^{II}(\pi'^{,n-1})$. However, the magnitude of the difference in f^{II} between the n signal bundle and its $n-1$ signal bundle induced by $\Re_x$ deletion is the same for π' and π^* and equals to

$$\Delta = \sqrt{\Re_l + \Re_x} + \sqrt{\Re_r + \Re_x} - \sqrt{\Re_l + \Re_r}.$$

Therefore

$$f^{II}(\pi^*) = f^{II}\left(\pi^{*,n-1}\right) + \Delta < f^{II}\left(\pi'^{,n-1}\right) + \Delta = f^{II}(\pi').$$

This is a contradiction to $f^{II}(\pi^*) > f^{II}(\pi')$ that followed from the non-optimality hypothesis of π^*.

Consider now the case where the triplet ($\Re_l$, $\Re_x$, $\Re_r$) does not exist in π'. Then there are two possibilities. In the first, the triplet appears in π' as a subsequence ($\Re_x$, max($\Re_l$, $\Re_r$), min($\Re_l$, $\Re_r$)). The pair swapping Property 3.1 can be applied on quadruple ($\Re$, $\Re_x$, max($\Re_l$, $\Re_r$), min($\Re_l$, $\Re_r$)) and result quadruple ($\Re$, max($\Re_l$, $\Re_r$), $\Re_x$, min($\Re_l$, $\Re_r$)), hence f^{II} can be reduced. In the second possibility, in any order at least one of $\Re_l$ and $\Re_r$ is a local maximum in π', say $\Re_l$. Then applying the local maximum elimination Property 3.3 to $\Re_l$ and moving it to be adjacent to $\Re_x$, will decrease f^{II} value of the newly created order. This again contradicts the optimality assumption of π'. □

Notice that although wire width W was uniform and predetermined, it can still be optimally set together with the spaces ($S_0,\ldots,S_n$) between the wires in order to minimize the total sum of delays, thus adding one more equation to (3.1)–(3.3). This is a simplification of the total sum of delays minimization problem [6], where individual wires may have different widths ($W_1,\ldots,W_n$).

3.2. Non-uniform wire widths implied by impedance matching

In the following we'll prove the optimality of the symmetric hill ordering for more general cases with non-uniform wire width. We assume that wire widths are matched to driver strengths, a common design practice in most practical VLSI designs. It is shown below that minimal total weighted sum of delays is obtained by symmetric hill ordering.

Let $\psi(R)$ be a positive, non-decreasing function of the driver resistance R, and let the corresponding wire width be defined by

$$W = 1/\psi(R). \tag{3.9}$$

In the former discussion of uniform wire width $\psi(R)$ was simply a constant. The relation in (3.9) represents impedance matching, where a stronger driver (smaller R) is assigned a wider wire with a lower impedance. According to (3.9), the effective signal resistance becomes $\Re = \alpha(d\psi(R) + hR)$. Then the following theorem can be stated:

Theorem 3.2. *(Optimal ordering of variable-width wires): Let a signal bundle have arbitrary drivers, arbitrary capacitive loads and wire width inversely proportional to the corresponding driver resistance. Then the symmetric hill ordering of the signals in the bundle according to effective signal resistances yields minimum total weighted sum of delays.*

Proof. All properties of symmetric hill order still hold since f^{II} remains an SRS. □

The function $\psi(R) = \alpha + \beta R$, where α and β are real positive number is admissible, providing further minimization compared to the case of uniform width. The minimum total sum of delays is obtained by first ordering the signals according to Theorem 3.2. Then a minimization of total sum of delays for that order takes place, where the wire spacing ($S_0,\ldots,S_n$) and the parameters α and β are the optimization variables. Notice that $\beta = 0$ is the case of uniform wire width.

3.3. Symmetric hill order for arbitrary wire width

Assume now that wire width can vary arbitrarily. It is no longer true that symmetric hill ordering yields the minimum total sum of delays. This general case might be caused by large capacitive loads, since the optimal setting of wire width depends on the corresponding load. This in turn affects the optimal order within the bundle. Note that if wire widths are predetermined ordering by effective driver resistance is still advantageous and the optimal order is unaffected by the capacitive loads.

What is the most general setting of wire widths such that symmetric hill order still yields minimal total weighted sum of delays? It can be derived by writing the relation between wire widths and driver resistances at minimum total sum of

delays. At the minimum, Eqs. (2.1) and (2.5) satisfy:

$$\frac{\partial f}{\partial W_i}+\lambda\frac{\partial g}{\partial W_i}=0,\quad 0\leqslant i\leqslant n-1. \tag{3.10}$$

Differentiating (2.1) and (2.5) we obtain

$$\frac{\partial f}{\partial W_i}=-\frac{\alpha_i}{W_i^2}\left(b+\frac{d}{S_i}+\frac{d}{S_{i+1}}+eC_i\right)+\alpha_i kR_i\quad \frac{\partial g}{\partial W_i}=1. \tag{3.11}$$

Substituting (3.11) into (3.10) yields

$$W_i=\sqrt{\frac{\alpha_i}{\lambda+k\alpha_i R_i}\left(b+\frac{d}{S_i}+\frac{d}{S_{i+1}}+eC_i\right)}. \tag{3.12}$$

Eq. (3.12) demonstrates the dependency between wire width at minimum total sum of delays and the corresponding driver resistance, spacing to adjacent wires, signal criticality and the capacitive load. Substitution of (3.12) into the expression for effective signal resistance presented in Definition 3.1 yields:

$$\Re_i=d\sqrt{\frac{\alpha_i(\lambda+k\alpha_i R_i)}{b+d/S_i+d/S_{i+1}+eC_i}}+\alpha_i hR_i. \tag{3.13}$$

Whenever $R_i\geqslant R_j$ implies $\Re_i\geqslant\Re_j$, symmetric hill order according to wire driver resistances yields minimum total sum of weighted delays among all possible orders.

As can be seen from (3.13), in order to satisfy the required relation in the numerator, $R_i\geqslant R_j$ should imply $\alpha_i\geqslant\alpha_j$, namely, the weaker the driver is, the more critical the signal is. For the term $d/S_i+d/S_{i+1}$ at the denominator it has been shown in (3.5) that optimality implies that the spaces are necessarily monotonically increasing with driver resistance, which also imposes a non-decreasing relation between $\Re_i$ and R_i. The only term remaining "free" is the capacitive load at the denominator of (3.13). In order to obtain a monotonic relation in (3.13) the following condition between resistance of drivers, their corresponding capacitive loads and signal criticality weights is imposed:

Theorem 3.3. *(Sufficient conditions for optimality of symmetric hill order): Let a n signal bundle have arbitrary drivers and capacitive loads. Let σ_i, σ_j, $0\leqslant i,j\leqslant n-1$ be any two signals and let (R_i, C_i, α_i) and (R_j, C_j, α_j) be their driver resistance, capacitive load and signal criticality weight, respectively. If the relation $R_i\geqslant R_j$ implies $C_i\leqslant C_j\wedge\alpha_i\geqslant\alpha_j$, then symmetric hill order according to driver resistances yields minimum total sum of weighted delays among all orders.*

Proof. If follows from Eq. (3.13) that if $R_i\geqslant R_j$ implies $C_i\leqslant C_j\wedge\alpha_i\geqslant\alpha_j$, then $\Re_i\geqslant\Re_j$. We can therefore replace the "effective driver resistance" phrase in Theorem 3.1 by "driver resistance" and obtain the same result. □

A special case of the Theorem 3.3 occurs in real design when all signals are of same criticality, at "first order" circuit implementation. In that case if $R_i\geqslant R_j\wedge C_i\leqslant C_j$, $0\leqslant i,j\leqslant n-1$, symmetric hill ordering is optimal and sizing optimization should be performed in this order. The true criticality of the signals due to the physical realization is then discovered. As a result the signals are assigned criticality weights according to how far is their delay from the requirement, and the signal order in the bundle is then verified to be in symmetric hill order according to (3.13). If relation (3.13) is not satisfied, the signals are reordered to satisfy symmetric hill, and wire resizing takes place again.

4. Implications of *MCF*

So far we ignored crosstalk effects between wires by assuming $MCF=1$. In order to account for worst-case wire switching, the cross capacitances should be multiplied by MCF values. Thus, the delay equation in (2.5) turns to be

$$\begin{aligned}f_3(\pi,\bar{W},\bar{S})&=\sum_{i=0}^{n-1}\alpha_i\Delta_i(\pi,\bar{W},\bar{S})\\&=\sum_{i=0}^{n-1}\alpha_i\Big\{a+R_i(kW_i+g+C_i)\\&\quad+\frac{b+eC_i}{W_i}+\left(hR_i+\frac{d}{W_i}\right)\left(\frac{MCF_i}{S_i}+\frac{MCF_{i+1}}{S_{i+1}}\right)\Big\},\end{aligned} \tag{4.1}$$

where MCF_i is Miller coupling factor between wires $i-1$ and i (for side wires it is the MCF between the wire and the sidewall). In practice, worst-case crosstalk effect on delays is usually represented by $MCF_i=2$ for $1\leqslant i\leqslant n-1$. If sidewall shielding wires are inactive, they do not induce Miller effect, i.e. $MCF_0=MCF_n=1$. Denoting MCF_{int} for all $0<i<n-1$ and MCF_{side} for $i=0$ and $i=n$, (4.1) can be rewritten as follows:

$$\begin{aligned}f_3(\pi,\bar{W},\bar{S})&=\sum_{i=0}^{n-1}\alpha_i\Delta_i(\pi,\bar{W},\bar{S})\\&=MCF_{\text{int}}\Bigg[\sum_{i=1}^{n-2}\alpha_i\Big\{a+R_i(kW_i+g+C_i)\\&\quad+\frac{b+eC_i}{W_i}+\left(hR_i+\frac{d}{W_i}\right)\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right)\Big\}\\&\quad+\alpha_0\Big\{a+R_0(kW_0+g+C_0)\\&\quad+\frac{b+eC_0}{W_0}+\left(hR_0+\frac{d}{W_0}\right)\left(\frac{MCF_{\text{side}}/MCF_{\text{int}}}{S_0}+\frac{1}{S_1}\right)\Big\}\\&\quad+\alpha_{n-1}\Big\{a+R_{n-1}(kW_{n-1}+g+C_{n-1})+\frac{b+eC_{n-1}}{W_{n-1}}\\&\quad+\left(hR_{n-1}+\frac{d}{W_{n-1}}\right)\left(\frac{1}{S_{n-1}}+\frac{MCF_{\text{side}}/MCF_{\text{int}}}{S_n}\right)\Big\}\Bigg].\end{aligned}$$

Decomposing f_3 into order independent and dependent components, the order dependent component is the following:

$$f^{\text{II}}=\frac{MCF_{\text{int}}}{A-nW}\left[\sum_{i=0}^{n-2}\sqrt{\Re_i+\Re_{i+1}}+\sqrt{r\Re_0}+\sqrt{r\Re_{n-1}}\right]^2, \tag{4.2}$$

where $r = MCF_{side}/MCF_{int}$ is called *MCF* ratio. If worst-case crosstalk is assumed between internal wires, then $r = 1/2$. The following shows that the order of wires which minimizes the total weighted sum of delays is *ascending*, where wires with strongest and weakest drivers are placed oppositely near the walls and all others are sorted monotonically between them (Fig. 1(c)). Before proving optimality of the ascending order, a few more properties are in order(Fig. 4).

Property 4.1. *End value repositioning for MCF ratio = 1/2*: let $(\Re_0,\ldots,\Re_{n-1})$ be a sequence of positive real numbers and $(\Re_i, \Re_{i+1})$ a pair of successive entries. If $\Re_i \leqslant \Re_0 \leqslant \Re_{i+1}$ (similarly $\Re_i \leqslant \Re_{n-1} \leqslant \Re_{i+1}$), then repositioning $\Re_0$ (similarly $\Re_{n-1}$) in between $\Re_i$ and $\Re_{i+1}$ decreases the SRS of the sequence (Fig. 4).

Proof. We need to show that

$$\sqrt{\tfrac{1}{2}\Re_0} + \sqrt{\Re_0 + \Re_1} + \sqrt{\Re_i + \Re_{i+1}} \geqslant \sqrt{\tfrac{1}{2}\Re_1} + \sqrt{\Re_i + \Re_0} + \sqrt{\Re_0 + \Re_{i+1}}.$$

Denote $p = \Re_1/\Re_0$, $q = \Re_i/\Re_0 \leqslant 1$, $r = \Re_{i+1}/\Re_0 \geqslant 1$, then the inequality turns into $\sqrt{\frac{1}{2}} + \sqrt{1+p} + \sqrt{q+r} \geqslant \sqrt{\frac{1}{2}p} + \sqrt{q+1} + \sqrt{1+r}$. Rearranging, we obtain $\sqrt{\frac{1}{2}} + \sqrt{1+p} - \sqrt{\frac{1}{2}p} \geqslant \sqrt{q+1} + \sqrt{1+r} - \sqrt{q+r}$. The left-hand side is minimized for $p = 0$. The right-hand size is monotonic increasing in q, thus maximized for $q = 1$. Therefore, if the inequality still holds for minimal left-hand side and maximal right-hand side, it always holds. Indeed, substituting $p = 0$ and $q = 1$ yields $\sqrt{1/2} + \sqrt{1} \geqslant \sqrt{2} + \sqrt{1+r} - \sqrt{1+r}$, which is definitely true. □

We show next the existence of optimal insertion for the case of *MCF* ratio = 1/2.

Property 4.2. *Optimal insertion for MCF ratio = 1/2*: Let $(\Re_0,\ldots,\Re_{n-1})$ be a sequence of ascending positive real numbers, let $\Re > \Re_{n-1}$. Then the location where inserting $\Re$ into the sequence minimizes the new SRS, is between $\Re_{n-1}$ and the wall. Hence the new sequence is also ascending.

Proof. Let us examine all $n+1$ possible locations for $\Re$ insertion. It follows from the pair swapping Property 3.1 that among the $n-1$ locations of which are not adjacent to walls, the best one is between $\Re_{n-1}$ and $\Re_{n-2}$. If we show that positioning $\Re$ between $\Re_{n-1}$ and the wall yields smaller SRS, we are done. We therefore need to show that $\sqrt{\Re_{n-2} + \Re} + \sqrt{\Re + \Re_{n-1}} + \sqrt{\frac{1}{2}\Re_{n-1}} \geqslant \sqrt{\Re_{n-2} + \Re_{n-1}} + \sqrt{\Re_{n-1} + \Re} + \sqrt{\frac{1}{2}\Re}$. Denote $p = \Re_{n-2}/\Re_{n-1} \leqslant 1$, $q = \Re/\Re_{n-1} \geqslant 1$. Substitution in the above inequality yields $\sqrt{p+q} + \sqrt{\frac{1}{2}} \geqslant \sqrt{p+1} + \sqrt{\frac{1}{2}q}$. Rearranging, we obtain $\sqrt{p+q} - \sqrt{\frac{1}{2}q} \geqslant \sqrt{p+1} - \sqrt{\frac{1}{2}}$. The left-hand side is monotonic increasing in q, so if we prove that the inequality holds for the minimal value of q, regardless of p, the inequality will always hold. Substitution of $q = 1$ in the inequality yields $\sqrt{p+1} - \sqrt{1/2} \geqslant \sqrt{p+1} - \sqrt{1/2}$, which is indeed true, independent of p(Fig. 5).

It remains to show that positioning $\Re$ between $\Re_0$ and the wall is inferior compared to positioning $\Re$ between $\Re_{n-1}$ and the wall. In terms of SRS, this translates to showing that $\sqrt{\frac{1}{2}\Re_{n-1}} + \sqrt{\Re_0 + \Re} + \sqrt{\frac{1}{2}\Re} \geqslant \sqrt{\frac{1}{2}\Re} + \sqrt{\Re + \Re_{n-1}} + \sqrt{\frac{1}{2}\Re_0}$. Denote $p = \Re_0/\Re_{n-1} \leqslant 1$, $q = \Re/\Re_{n-1} \geqslant 1$. Substitution yields $\sqrt{\frac{1}{2}} + \sqrt{p+q} \geqslant \sqrt{q+1} + \sqrt{\frac{1}{2}p}$. Rearranging, we obtain $\sqrt{\frac{1}{2}} + \sqrt{p+q} - \sqrt{\frac{1}{2}p} \geqslant \sqrt{q+1}$. The left-hand side is monotonic decreasing

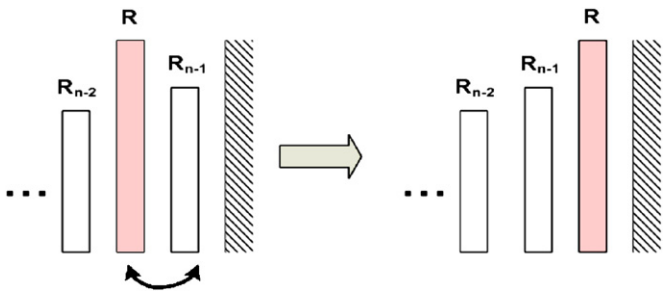

Fig. 5. End value repositioning.

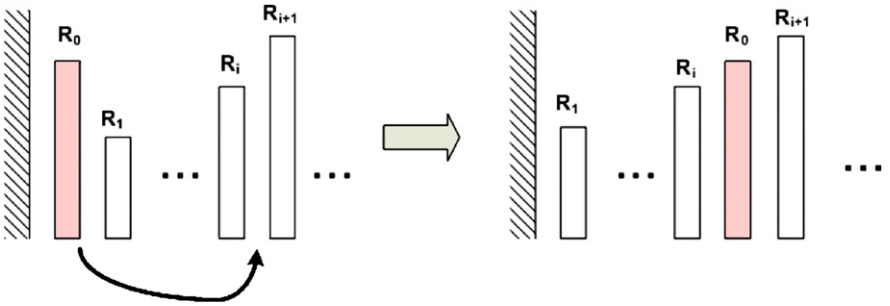

Fig. 4. Optimal insertion case: the location near the wall is better than the location between two largest values.

in p, which follows from $\partial/\partial p\left(\sqrt{\frac{1}{2}}+\sqrt{p+q}-\sqrt{\frac{1}{2}p}\right)=\left(1/2\sqrt{p+q}\right)-\left(1/2\sqrt{2p}\right)\leqslant\left(1/2\sqrt{p+p}\right)-\left(1/2\sqrt{2p}\right)=0$. Therefore, if the inequality holds at minimum of left-hand side, it always holds. Substituting $p=0$ we obtain $\sqrt{1/2}+\sqrt{q}\geqslant\sqrt{q+1}$, which is always true for $q\geqslant 1$. □

The above properties establish the theorem below.

Theorem 4.1. *(Optimal ordering with MCF ratio = 1/2)*: Let a signal bundle have arbitrary drivers, arbitrary capacitive loads, wire width decreasing with the corresponding driver resistance and *MCF* at walls 1/2 of *MCF* between wires inside the bundle. Then ascending order of the signals in the bundle according to effective signal resistances yields minimum total weighted sum of delays.

Proof. Let $\pi^*=(\Re_0,\ldots,\Re_{n-1})$ be sorted left to right in ascending order, and let $f^{\mathrm{II}}(\pi^*)$ be the corresponding term in the total sum of delays which depends on the SRS. We'll show by induction that for any other ordering π of driver resistances $f^{\mathrm{II}}(\pi^*)\leqslant f^{\mathrm{II}}(\pi)$.

For a bundle comprised of one or two signals the induction hypothesis trivially exists. For a bundle of three signals, the optimality of ascending order follows from the *optimal insertion property*. By the induction hypothesis, ascending order is optimal for any $n-1$ signals bundle. Assume on the contrary that there exists a n signal bundle whose optimal order π' is not ascending. It follows from the non-optimality contradictory hypothesis that $f^{\mathrm{II}}(\pi^*)>f^{\mathrm{II}}(\pi')$.

Consider the location of the successive pair $(\Re_{n-2},\Re_{n-1})\subset\pi^*$ in π'. It certainly cannot occur next to the right side wall. Because if it did, then $\Re_{n-1}$ can be dropped from both π^* and π'. The remaining part of π^*, $\pi^{*,n-1}$, is ascending ordered, while the remaining part of π', $\pi'^{,n-1}$, is not. SRS in both $\pi^{*,n-1}$ and $\pi'^{,n-1}$ is decreased by $\delta=\sqrt{\frac{1}{2}\Re_{n-1}}-\sqrt{\frac{1}{2}\Re_{n-2}}+\sqrt{\Re_{n-2}+\Re_{n-1}}$. On the other hand, it follows from the induction hypothesis that $\pi^{*,n-1}$ is an optimal order, while $\pi'^{,n-1}$ is not, thus implying that $f^{\mathrm{II}}(\pi^{*,n-1})<f^{\mathrm{II}}(\pi'^{,n-1})$. Consequently, $f^{\mathrm{II}}(\pi^*)=f^{\mathrm{II}}(\pi^{*,n-1})+\delta<f^{\mathrm{II}}\left(\pi'^{,n-1}\right)+\delta=f^{\mathrm{II}}(\pi')$, thus contradicting $f^{\mathrm{II}}(\pi^*)>f^{\mathrm{II}}(\pi')$.

The above shows that it is impossible for an optimal ordering to have the pair $(\Re_{n-2},\Re_{n-1})$ residing next to the right wall (unless this is the ascending order π^*, which we aim to prove is optimal). We'll show next that any order π' claiming to be optimal must have $\Re_{n-1}$ positioned next to the right wall, by showing that if this was not the case, we could always decrease the corresponding SRS by changing the position of one of the other $\Re$'s.

Indeed, if this was not the case, let $\Re^{\min}=\min_{0\leqslant i\leqslant n-2}\Re_i$. Assume that $\Re^{\min}$ is located in π' between $\Re_{n-1}$ and the left wall, as shown in Fig. 6. (If $\Re^{\min}$ is located in π' between $\Re_{n-1}$ and the right wall, we could have mirrored the order since SRS is invariant over mirroring of $\Re$'s order). Pick $\Re'$ which is located next to the right wall. Let $\Re''$ be the rightmost located between $\Re_{n-1}$ and the left wall such that $\Re''\leqslant\Re'\leqslant\Re_{n-1}$, as shown in Fig. 6. Such $\Re''$ must exist since $\Re^{\min}\leqslant\Re'\leqslant\Re_{n-1}$. Let $\Re'''$ be located next to $\Re''$ on its right side as shown in Fig. 6. It follows from the way we selected $\Re'$ and $\Re''$ that $\Re''\leqslant\Re'\leqslant\Re'''$. We can now apply the properties of end value repositioning for *MCF* ratio $\frac{1}{2}$ and reposition $\Re'$ between $\Re''$ and $\Re'''$, thus decreasing the corresponding SRS. Such decrement could not happen if $\Re_{n-1}$ would have been located next to the right wall.

But having $\Re_{n-1}$ necessarily located next to the right wall implies that $\Re_{n-2}$ must be left adjacent to $\Re_{n-1}$, since if this was not the case we could apply again the properties of end value repositioning and pair swapping and insert $\Re_{n-2}$ between $\Re_{n-1}$ and its left adjacent $\Re$.

In summary, we've shown that any order aiming at minimizing SRS for *MCF* ratio 1/2 must have $(\Re_{n-2},\Re_{n-1})$ next to the right wall. Consequently, the ascending order is superior over any other ordering having $(\Re_{n-2},\Re_{n-1})$ next

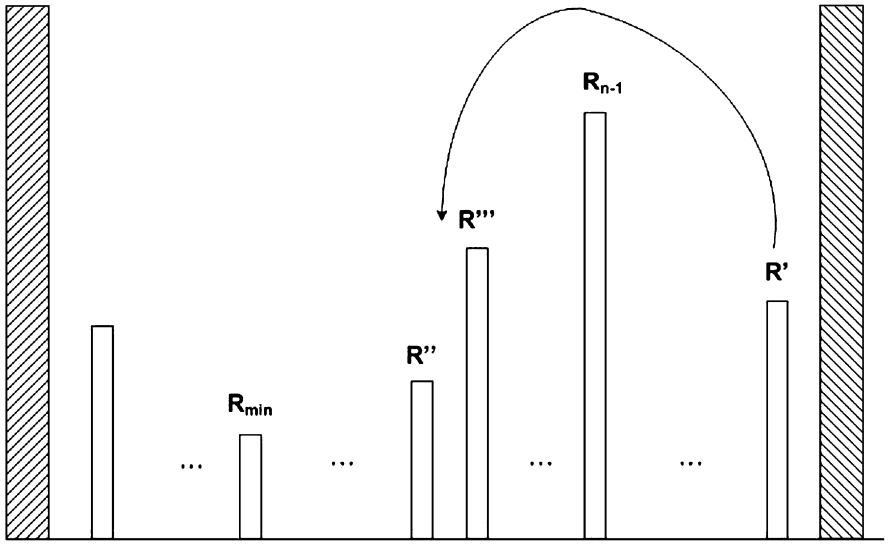

Fig. 6. Proof of optimal ordering with *MCF* ratio = 1/2.

to right wall as already shown, which concludes the proof. Similar arguments hold for the case where the pair ($\Re_{n-1}$, $\Re_{n-2}$) is positioned next to the left wall. □

Consider now the case where the *MCF* occurring between the end signals and the walls is zero. This case corresponds to active shielding [4]. Therefore, the *MCF* ratio between the end signals and the internal ones is zero. In the following we'll show that the order of effective drivers yielding the smallest SRS is such that the two signals having weakest drivers are located near the walls, one at each side. The strongest one is located at the center. The rest are evenly and symmetrically distributed on both sides in ascending order of their effective driver strength, from the ends towards the center. Such an order is called *symmetric valley*, defined formally as follows.

Definition. *Symmetric valley ordering*: Let $\Re_0 \leqslant \Re_1 \leqslant, \cdots, \leqslant \Re_{n-2} \leqslant \Re_{n-1}$ be a sequence of n positive real numbers increasingly ordered. Assume without loss of generality that n is even. Let us split it into even and odd interleaved subsequences $\Re_0 \leqslant \Re_2 \leqslant, \cdots, \leqslant \Re_{n-2}$ and $\Re_1 \leqslant \Re_3 \leqslant, \cdots, \leqslant \Re_{n-1}$. Reverse the order of numbers in the odd subsequence, thus turning it into monotonic decreasing sequence. Finally, concatenate the odd and the modified (reversed) even subsequences into one sequence. The new sequence thus obtained is said to be ordered in *symmetric valley ordering* (as it resembles descending and climbing a symmetric valley). Fig. 7 illustrates how such an order is obtained. The following property is analogous to *optimal insertion of maximal value* 3.2 derived for *symmetric hill order*.

Property 4.1. *Optimal insertion of minimal value*: Let $(\Re_0, \ldots, \Re_{n-1})$ be a sequence of positive real numbers ordered as a symmetric valley. Let $\Re < \min\{\Re_0, \ldots, \Re_{n-1}\}$. Then the location where inserting $\Re$ into the sequence minimizes the new SRS, is at the center between the two smallest numbers. Hence the new sequence is also in symmetric valley order.

We skip the proof of this property, as it follows similarly to the proof of *optimal insertion of maximal value* 3.2. The following theorem manifests the optimal ordering for 0 *MCF* ratio.

Theorem 4.2. *(Optimal ordering with MCF ratio = 0): let a signal bundle has arbitrary drivers, arbitrary capacitive loads and wire width decreasing with the corresponding driver resistance. Let the MCF at the side walls be 0 and MCF of wire pairs inside the bundle be equal to all. Then, the symmetric valley order of the signals in the bundle according to effective driver resistances yields minimum total weighted sum of delays.*

Proof. Like the case of *MCF* ratio 1, where the optimal order is symmetric hill, the pair swapping Property 3.1 and local maximum elimination Property 3.3 hold also for this case, since both involve comparing SRS of internal signals only. Following similar arguments as in symmetric hill order, with the aid of *optimal insertion of minimal value* Property 4.1, the proof is identical to Theorem 3.1. □

Theorems 3.1, 4.1 and 4.2 manifested the optimal signal ordering in a bundle for typical cases of *MCF* boundary conditions, where external to internal signal *MCF* ratios are 1, $\frac{1}{2}$ and 0. The implied orders are independent of the effective drivers' strengths and are valid under very wide wire width settings applicable for most practical design scenarios. An interesting question is what happens for other *MCF* ratios. With some further manipulations of SRS it can be shown that:

- When the ratio of end *MCF* to internal *MCF* is equal or greater than 1, *symmetric hill* order yields minimal total weighted sum of delays, independently of effective drivers' strength.
- When the ratio of end *MCF* to internal *MCF* is equal to $\frac{1}{2}$, *ascending* order yields minimal total weighted sum of delays, independently of effective drivers' strength.
- When the ratio of end *MCF* to internal *MCF* is equal to or smaller than 0 *symmetric valley* order yields minimal total weighted sum of delays, independently of effective drivers' strength.

For all other ratios, namely, $0 < r < 1/2$and $1/2 < r < 1$ the order depends on the specific values of effective drivers' strength and may be none of the above.

5. Crosstalk noise reduction

Instead of incorporating delay uncertainty into the delay expression by using worst-case Miller factor, we may directly consider delay uncertainty and optimize it simultaneously with the nominal (crosstalk-free) signal delay.

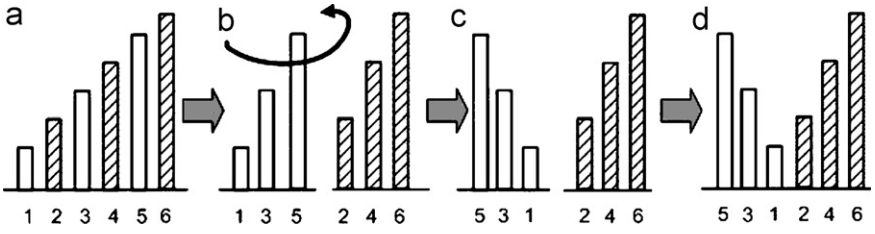

Fig. 7. Construction of symmetric valley ordering: (a) sort numbers in ascending order; (b) split sequence into odd and even subsequences; (c) reverse order of numbers in the odd subsequence; (d) concatenate the even and the modified subsequences.

For calculating crosstalk noise effectively, several models have been presented in the literature, e.g. [17,26]. For peak noise voltage V^p we use a simple model, given in [17]. The peak noise in wire i can be represented as

$$V_i^p = V_{dd}\frac{R_i C_{c_i} + R_{w_i} C_{c_i}/2}{\Delta_{i-1} + \Delta_i + \Delta_{i+1}}. \quad (5.1)$$

In (5.1), the numerator represents a part of wire delay caused by coupling capacitance, and the denominator represents the sum of Elmore delays of the wire and its neighbors. Rewriting (5.1) in terms of (2.2), obtain

$$V_i^p = V_{dd}\frac{(d/W_i + hR_i)(1/S_i + 1/S_{i+1})}{\Delta_{i-1} + \Delta_i + \Delta_{i+1}}, \quad 0<i<n-1,$$
$$V_0^p = V_{dd}\frac{(d/W_0 + hR_0)1/S_1}{\Delta_0 + \Delta_1},$$
$$V_{n-1}^p = V_{dd}\frac{(d/W_{n-1} + hR_{n-1})1/S_{n-1}}{\Delta_{n-1} + \Delta_n}. \quad (5.2)$$

For analytical modeling of the delay uncertainty caused by effects of crosstalk noise on circuit timing, we use superposition-based approximations, proposed in [27]. According to the approximation, the upper bound of delay uncertainty of wire i can be expressed as

$$\delta_{\max,i} = \Delta_i \ln(2V_i^p/V_{dd} + 1). \quad (5.3)$$

Let us introduce two new objective functions:

$$h_1 = \sum_{i=0}^{n-1} \delta_{\max,i} \quad (5.4)$$

and

$$h_2 = \max_i \delta_{\max,i}, \quad (5.5)$$

which are the total sum of delay uncertainties and the largest delay uncertainty among the wires in the bundle.

According to [28], after some simplifications (5.2) can be represented in the form $V_i^p \approx V_{dd}(R_i/(R_{i-1} + R_i + R_{i+1}))\eta$, where η represents the ratio of cross-coupling capacitance to total wire capacitance.

As it follows from this expression, if the driver of a wire is significantly larger than the driver of its neighbors, then the wire with the smaller driver (as a crosstalk victim) will be exposed to serious noise from the wires with the larger drivers (aggressors). Therefore, crosstalk noise will be minimized, if neighboring wires have roughly equal drivers [28]. It can be achieved by ordering wires in the bundle in one of the monotonic orders discussed above.

Although we have not performed direct mathematical optimization of delay uncertainty, our experiments have shown that total delay uncertainty (5.4) is reduced by minimizing the total weighted sum of delays (2.4), and the worst delay uncertainty (5.5) is reduced by minimization the worst wire delay (2.3), using a symmetric hill order.

6. Experimental results

Numerical experiments for various problem instances were performed using 65 nanometer technology parameters. Continuous optimization has been used, and results were verified for allowed discrete sizes as required by the technology. Delay improvements were verified by SPICE simulations of several circuits before and after optimization.

In all experiments we assume uniform timing requirements, unless mentioned otherwise.

Experiment 1. This experiment demonstrates the benefit of wire ordering. Random problem instances using five signals were evaluated as follows: Each signal was assigned a driver randomly. The range of driver resistances was 50 Ω to 3 kΩ, and load capacitances in the range 10–200 fF were assigned according to driver strength to avoid excessive driver loading, such that the conditions of Theorem 3.3 were always satisfied. For each problem the wire widths and spaces were optimized once to yield minimum total sum of delays, and again to yield minimum worst-wire delay (MinMax). This was repeated for all the $5! = 120$ possible orders. The procedure was done for eight different

Table 1
Average improvement (best vs. worst ordering) for random problem instances, in sum-of-delays (upper half cell) and worst wire delay (lower half cell)

Bundle length (μm)	Bundle width							
	1.5 μm (%)	2 μm (%)	2.5 μm (%)	3 μm (%)	3.5 μm (%)	7 μm (%)	9.5 μm (%)	12 μm (%)
300	10.14	9.13	8.13	7.25	6.62	3.12	2.25	1.97
	17.19	14.98	12.7	10.86	9.84	4.6	2.86	2.13
500	11.31	9.5	8.21	7.46	6.71	3.32	2.43	2.14
	17.24	15.18	13.29	10.81	9.64	5.13	3.07	2.94
800	9.82	8.76	7.79	7.32	6.5	2.47	1.92	1.05
	16.22	14.11	13.08	11.09	9.98	5.14	3.24	1.83
1200	8.78	8.23	7.38	6.89	6.35	2.24	1.7	1.1
	14.18	14.58	13	11.63	9.84	5.13	2.72	1.51
1500	7.63	7.2	6.94	6.54	6.12	2.1	1.81	0.97
	14.13	14.02	12.97	11.51	10.15	4.99	2.62	2

bundle widths A—1.5, 2, 2.5, 3, 3.5, 7, 9.5 and 12 μm, and five different bundle lengths L—300, 500, 800, 1200 and 1500 μm. The optimization impact (% improvement of best versus worst ordering, after width/space optimization, averaged over 20 random problem instances for each width and length configuration) is presented in Table 1. This experiment demonstrates that net ordering can significantly improve results of wire sizing and spacing optimization, especially when the bundle width is tightly constrained. All obtained optimal orders for total sum of delays minimization came out as symmetric hills (as expected, since Theorem 3.2 is always satisfied in this example). As can be seen from the table, bundle worst wire delay (lower half cell) is more sensitive to the ordering than the total sum of delays (upper half cell).

Experiment 2. This experiment evaluates the benefit of ordering for a large number of wires in the bundle. The impact of net ordering on interconnect bundles containing a large number of wires was evaluated, using 15 representative interconnect bundles in 65 nm technology. The number of signal wires per bundle varied from 10 to 128. The width of each bundle was determined by allocating per wire four times the minimal width implied by the minimum design rules. Driver resistances varied from 50 Ω to 2.5 kΩ, averaging 1.24 kΩ. Exhaustive search to find the worst and best ordering is infeasible for such problems. Instead, a poor ordering has been guessed, and the corresponding signal delays were compared with results of symmetric hill ordering. The experiment confirmed that symmetric hill net ordering could improve delays by a significant percentage: After net ordering and sizing optimization, up to 18.3% in average delays were obtained. On average, the interconnect delay improvement in this experiment was 11.8%, which is equivalent to 5% of the clock cycle used in the given technology.

Experiment 3. This example demonstrates how the set of wire driver resistances influences the impact of ordering optimization. The effect of signal ordering on MinMax delay in bundles with both strong and weak drivers is shown in Table 2. A bundle of 7 signals with driver-load pairs of (50 Ω, 50 fF) or (3 kΩ, 5 fF) is examined for various numbers of the weak drivers. Bundle width and length were $A = 3$ μm and $L = 500$ μm. As can be expected, when the numbers of strong and weak drivers were about equal, signal ordering is most effective. The worst ordering is indeed the interleaved one, described in Fig. 2(a), while the best one is clearly symmetric hill.

Table 2
% Improvement of best versus worst ordering, after width/space optimization, for a signal channel with two driver strengths

No. of weak drivers	Percent of improvement in worst delay (%)
1	0.11
2	8
3	12.7
4	16.3
5	10.76
6	5.25

Experiment 4. This example demonstrates the influence of driver's resistances range on ordering optimization impact. The range of drivers is specified by the ratio R_{max}/R_{min}, where R_{max} and R_{min} are the largest and the smallest driver resistances in a set of wires being ordered. 19 different seven-wire sets were evaluated, with driver resistances distributed uniformly around a constant average of 1 kΩ. In these sets, R_{max}/R_{min} varied from 1 (all drivers equal) to 6.4. Bundle length is 700 μm and width is 3 μm in all cases. The results are presented in Fig. 8. As can be seen, optimization impact increases with resistance range. Worst wire delay optimization is influenced much more than optimization of average delay. For larger range of driver resistances, the increase in delay improvement saturates.

Experiment 5. This experiment demonstrates the impact of signal criticality weight. Consider a 3 μm-wide bundle of 500 μm length with five nets in it with drivers of different strengths, and all load capacitances are equal to 10 fF. The cross section of the bundle after sum-of-weighted-delays optimization when all nets have uniform timing requirements (all weights are 1) is shown in Fig. 9a. The wire with the largest driver (2.8 kΩ), is allocated the largest spaces, as expected. After ordering optimization, according to symmetric hill order by driver resistances, this wire is placed in the middle of the bundle (Fig. 9b). Assume now that the net with the strongest driver (0.05 kΩ) is the most critical and is assigned $\alpha = 10$. The situation after sum-of-weighted-delays optimization and ordering optimization are shown at Fig. 10a and b respectively. Now, the critical net is placed close to the middle and shares a large space with the weakest driven net. In both cases, the average weighted delay was reduced by about 8%. In the second case, the net with the strongest driver was allocated larger width in order to reduce wire resistance due to net criticality. The experiment shows that the weighted sum method takes into account simultaneously both wire driver resistance and net criticality.

Experiment 6. This experiment demonstrates a-priory assignment of wire widths by a heuristic that guarantees optimality of symmetric hill ordering. This is compared

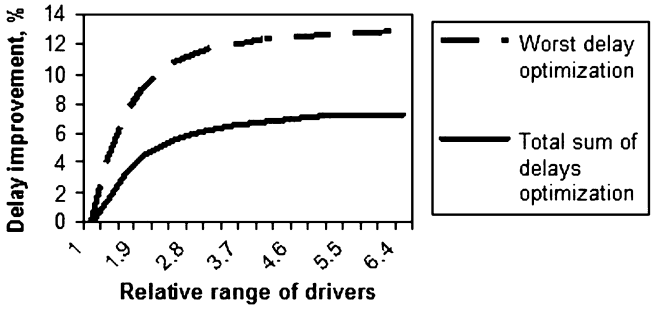

Fig. 8. Influence of relative range of drivers on optimization impact.

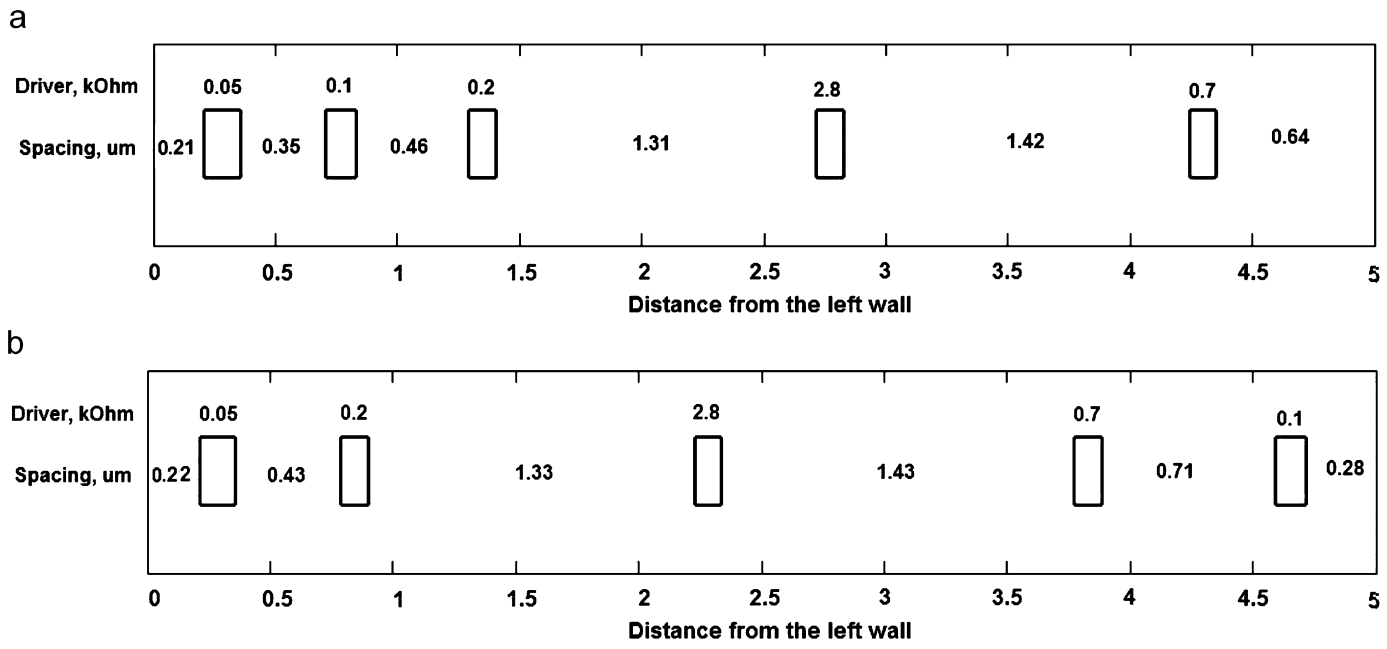

Fig. 9. A bundle with uniform timing requirements; (a) cross section after weighted sum minimization without ordering; (b) cross section after weighted sum of delays minimization with ordering (symmetric hill order according to driver resistances).

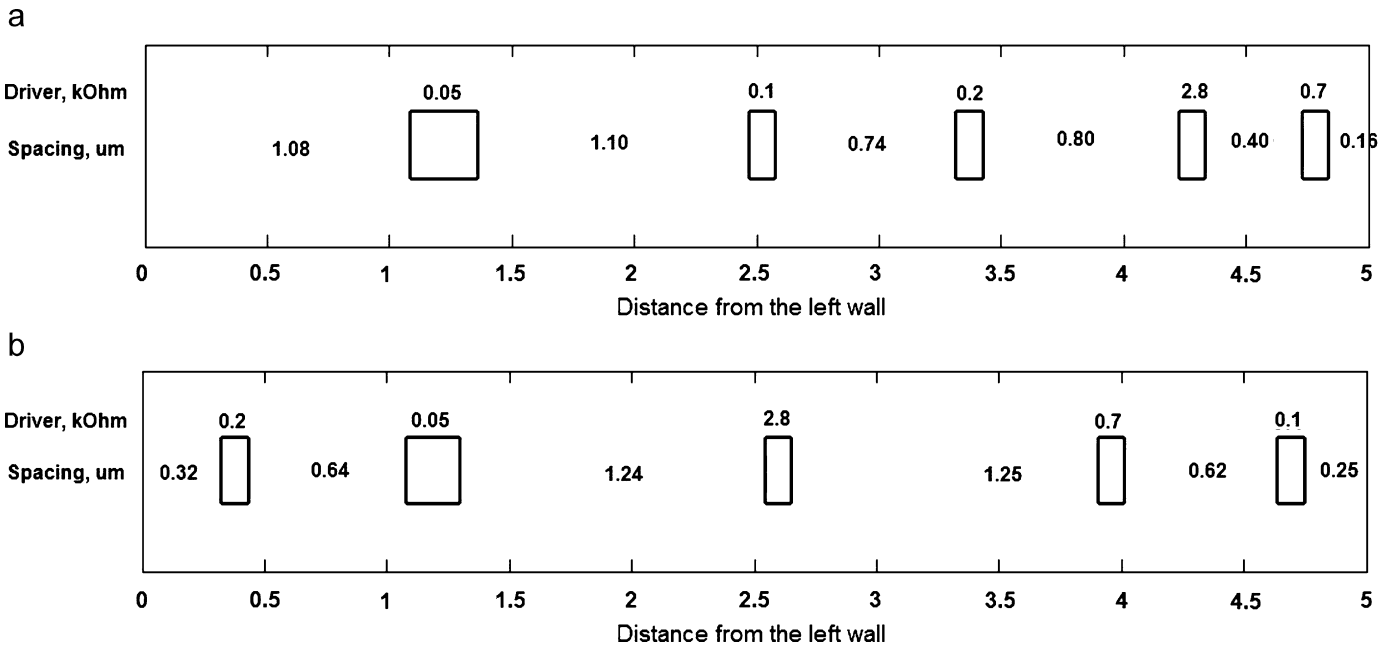

Fig. 10. A bundle with a critical wire; (a) cross section after weighted sum minimization without ordering (the critical wire is at the leftmost position); (b) cross section after weighted sum minimization with ordering (symmetric hill order according to effective signal resistance).

with the most general optimization where ordering, width and spacing are searched exhaustively. In this experiment, delays obtained by exhaustive simultaneous ordering/sizing/spacing optimization are compared with results of heuristics using symmetric hill order for total sum of delays objective. Another set of random 1600 instances was generated with the same range of drivers and the same set of bundle widths and lengths, but all load capacitances equal to 10 pF. Heuristic wire width assignment with the inverse linear width function $W = (1/(\alpha + \beta R))$ was applied. For each value of bundle width and length, the delay difference between the optimal result of exhaustive search and the result of the heuristic was expressed as a fraction of the delay difference between best and worst results of the exhaustive search. On average for all these problem instances, the global minimum delay was approached as closely as 0.37%. Hence, the heuristic wire width assignment, which

Table 3
Percent of average improvement in delay uncertainty (best vs. worst ordering) for random problem instances, obtained by sum-of-delays optimization (upper half-cell—average wire delay uncertainty, lower half-cell—worst wire delay uncertainty)

	$A = 2\,\mu m$	$A = 5\,\mu m$	$A = 8\,\mu m$	$A = 12\,\mu m$	$A = 20\,\mu m$
$L = 300\,\mu m$	21.9	27.1	28.8	31.3	38.6
	26.6	32.2	38.2	48.1	46.7
$L = 500\,\mu m$	22.1	26.9	28.4	30.6	32.6
	29.1	30.5	39.3	45.2	39.8
$L = 800\,\mu m$	22.8	28.6	28.7	32.5	33.8
	28.3	34.7	38.4	36.6	44.1
$L = 1200\,\mu m$	23.5	27.7	29.2	34.4	33.4
	25.3	30.7	37.0	41.2	38.9
$L = 1500\,\mu m$	24.1	27.6	29.9	34.4	29.3
	24.8	30.5	37.2	37.1	39.9

allows to use symmetric hill ordering instead of exhaustive search, is effective.

Experiment 7. In this experiment we demonstrate crosstalk reduction results by wire ordering. We evaluated 20 random problem instances using five signals. Each signal was assigned a driver randomly. The range of driver resistances was $100\,\Omega$ to $2\,k\Omega$ and load capacitances in the range 200–10 fF were assigned accordingly to satisfy Theorem 3.3. For each problem the wire widths and spaces were optimized twice: first to yield minimum total sum of delays, and second to yield minimum worst wire delay. This was done for all the $5! = 120$ possible order permutations. The procedure was repeated for five different bundle widths of 2, 5, 8, 12 and 20 μm, and five different lengths of 300, 500, 800, 1200 and 1500 μm. For the best and worst timing orders, the total sum of delay uncertainties and maximum delay uncertainty were calculated. The crosstalk results for total sum of delays optimization is presented in Table 3 (the results for worst wire delay optimization are very similar) In each cell, the upper half cell represents improvement in total sum of delay uncertainties and the lower half cell—improvement in maximum delay uncertainty. The experiment demonstrates that net ordering can significantly improve bundle noise immunity. The maximum delay uncertainty is affected more than sum of delay uncertainties.

7. Conclusion and open questions

Reordering of wires in a constrained-width interconnect bundle has been studied. It has been shown that a monotonic order of the signals according to their effective driver resistance yields the smallest average weighted delay among all possible orderings of signal wires. The weighted delay objective was chosen in order to approximate MinMax optimization. Three variants of monotonic ordering have been found to be optimal, depending on the *MCF* ratio between the signals at the sides of the bundle and that of the internal wires.

The monotonic order property exists for a very broad range of VLSI circuit settings arising in common design practice. The paper proposed a simple, yet near-optimal, setting of wire widths within the bundle to yield the best average weighted delay.

The above theoretical results have been validated by numerical experiments on 65 nm process technology and industrial design data. In all cases the ordering optimization yielded improvement in the range of 10% in wire delay, translated to about 5% improvement in the clock cycle of high-performance microprocessor implemented in that technology.

The authors could not prove that monotonic ordering by effective signal resistance yields the smallest MinMax timing slack, as it does for the average weighted delay. It is an interesting and important question what are the problem settings that ensure that monotonic ordering would yield the smallest MinMax delay.

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