Optimal Bus Sizing in Migration of Processor Design

Shmuel Wimer, Shay Michaely, Konstantin Moiseev, *Student Member, IEEE*, and Avinoam Kolodny, *Member, IEEE*

***Abstract*—The effect of wire delay on circuit timing typically increases when an existing layout is migrated to a new generation of process technology, because wire resistance and cross capacitances do not scale well. Hence, careful sizing and spacing of wires is an important task in migration of a processor to next generation technology. In this paper, timing optimization of signal buses is performed by resizing and spacing individual bus wires, while the area of the whole bus structure is regarded as a fixed constraint. Four different objective functions are defined and their usefulness is discussed in the context of the layout migration process. The paper presents solutions for the respective optimization problems and analyzes their properties. In an optimally-tuned bus layout, after optimizing the most critical signal delay, all signal delays (or slacks) are equal. The optimal solution of the MinMax problem is always bounded by the solution of the corresponding sum-of-delays problem. An iterative algorithm to find the optimally-tuned bus layout is presented. Examples of solutions are shown, and design implications are derived and discussed.**

***Index Terms*—Interconnections, integrated circuit layout, timing.**

I. Introduction

INTERCONNECT delays have become dominant in CMOS VLSI digital systems as a result of technology scaling [1], [2]. In recent generations, wire resistance and cross-capacitance between adjacent wires have become increasingly important in their effect on signal delay. For a given metal layer, wire resistance and cross-capacitance depend on wire width and inter-wire spacing, respectively. Allocation of wire widths and spaces for bus structures under a total area constraint is an important problem in process migration of existing mask layouts (also known as "process shifting"), which often produces excessive wire delays in the new layout. In state-of-the-art technology migration, about 10% improvement in timing of buses is achievable by judicious allocation of wire widths and inter-wire spaces. The strategy of allocating widths and spaces to maximize performance in bus structures was proposed in [3] without formal analysis and solution. The nature of this problem allows tradeoff between the resistance of a wire and its coupling capacitances to adjacent wires, by increasing wire width while reducing spaces, or vice versa. Wire resistance affects only the delay of the signal carried by the wire, while coupling capacitances affect the delays of both the wire and its neighbors. For multiple nets, the optimal solution involves simultaneous tradeoffs among all wires sharing a given common area.

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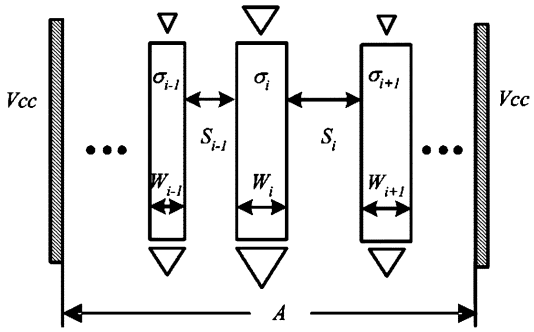

Fig. 1. Structure of the bus: n parallel signal wires share a fixed total width A between two shield wires.

The wire sizing problem has been addressed in [4] and [5] for a single wire and for a single-net interconnect tree. Simultaneous wire sizing and driver sizing has been presented in [6], [7]. The problem of sizing and spacing multiple nets with consideration of coupling capacitance in global interconnect has been addressed in [8], considering general tree structures for nets with fixed terminals, without a total area constraint. The authors modeled coupling between nets by converting cross-capacitance into an effective fringe capacitance, which resulted in a decoupled delay model for each net. The routing tree for each net was sized independently, using an algorithm based on dynamic programming [9]. Coupling capacitance has been considered more explicitly in the context of physical design algorithms for minimizing crosstalk noise [4], [10], [11] or dynamic power [12]. The authors of [13] derived layout guidelines and presented a simultaneous multiple-net spacing algorithm for area minimization in general layouts under a noise-constraint.

This paper addresses the problem of simultaneously assigning widths and spaces to n parallel wires, representing a bus or several interleaved busses, as illustrated in Fig. 1. Such geometry is commonly used in practice, and its simplicity enables straightforward mathematical analysis. With given drivers, load capacitances and timing requirements for the individual signals, wire widths and spaces are allocated to maximize circuit speed. Note that driver strengths, load capacitances and required arrival times are not necessarily equal. The total sum of widths and spaces is a given constraint, representing the total width available for the bus structure in the layout. The problem is presented in the context of technology migration, but the same methods can be used to optimize an initial design, not just a migrated one.

II. Problem Formulation

Consider a bus of n signal nets $\sigma_1, \ldots, \sigma_n$ between two sidewalls (wires at fixed locations, connected to V_{cc} or V_{ss}) as shown in Fig. 1. S_{i-1} and S_i, respectively, denote spaces to the right

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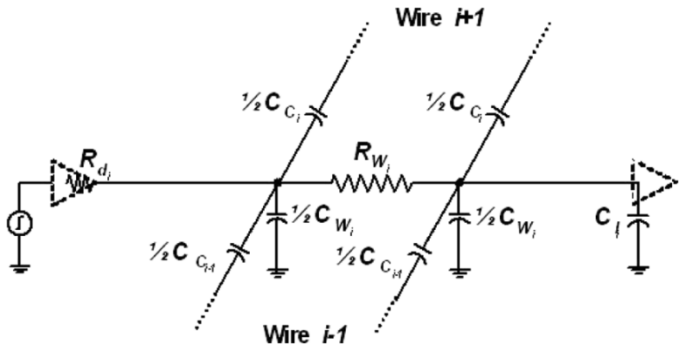


Fig. 2. Equivalent circuit for calculating the ith signal delay.

and left neighbors of wire W_i. The length of each wire is L. The sum of wire widths and spaces between the left and right side walls is given in the following constraint, which represents the total width A of the available area for laying out the signal bus

$$g(\overline{W},\overline{S}) = \sum_{j=1}^{n} W_i + \sum_{j=0}^{n} S_i = A. \tag{1}$$

Another set of constraints on wire sizing is geometrical design rules, which are imposed by the manufacturing technology. In modern processes of 90 nanometers and below, the width and the space of wires are bounded in some range as follows:

$$S' \le S_i \le S'', 0 \le i \le n, \text{ and} \tag{2}$$
$$W' \le W_i \le W'', 1 \le i \le n. \tag{3}$$

III. Delay Model

Signal delays are expressed by an Elmore model using simple approximation for capacitances. The delay of signal σ_i can be calculated from the π-model equivalent circuit shown in Fig. 2, where R_{d_i} is the effective output resistance of the driver, R_{w_i} is the wire resistance, C_{w_i} is the wire area and fringe capacitance, $C_{c_{i-1}}$ and C_{c_i} are coupling capacitances to the right and left neighboring signals, and C_{l_i} is the capacitive load presented by the receiver's input. Using technology parameters these can be expressed as $R_{R_i} = R_s L/W_i$, $C_{w_i} = C_a L W_i + C_f L$, and $C_{c_i} = k_c L/S_i$, where C_a is area capacitance coefficient, C_f is fringe capacitance coefficient, k_c is a line-to-line coupling coefficient, and R_s is the metal sheet resistance. These are first-order approximations [14] which capture the fundamental nature of the problem.

Under Elmore delay model, the delay Δ_i of signal σ_i from driver's input to receiver's input is given as follows:

$$\begin{aligned}\Delta_i = {} & R_{d_i} C_a L W_i + \left(D_i + R_{d_i} C_f L + R_{d_i} C_{l_i} + \frac{1}{2} C_a R_s L^2\right) \\ & + \left(\frac{1}{2} R_s C_f L^2 + R_s L C_{l_i}\right) \frac{1}{W_i} \\ & + R_{d_i} k_c L \left(\frac{MCF_{i-1}}{S_{i-1}} + \frac{MCF}{S_i}\right) \\ & + \frac{1}{2} R_s k_c L^2 \frac{1}{W_i} \left(\frac{MCF_{i-1}}{S_{i-1}} + \frac{MCF_i}{S_i}\right).\end{aligned} \tag{4}$$

Note that the cross-coupling capacitances between wires are multiplied by a Miller coupling factor (MCF) [16] in the model equation. For nominal delays, without delay uncertainty induced by crosstalk, $\mathrm{MCF} = 1$ is assumed. This is valid in particular when adjacent wires are functionally interleaved, such that simultaneous transitions of neighbor wires are avoided. If all wires can switch simultaneously, the cross-capacitance terms are typically multiplied by a uniform MCF of 2. For such a case, inter-wire tradeoffs would become even more pronounced in optimizing the bus layout. In the remainder of this paper we assume $\mathrm{MCF} = 1$. The coefficients of wire width and spaces in (4) will be marked as a_i, b_i, c_i, d_i, e. The delay expression can be rearranged as

$$\Delta_i(\overline{W},\overline{S}) = a_i W_i + b_i + \frac{c_i}{W_i} + \left(d_i + \frac{e}{W_i}\right) \times \left(\frac{1}{S_{i-1}} + \frac{1}{S_i}\right). \tag{5}$$

Note that in (5), the coefficient e is not indexed since it encapsulates only technology parameters, which are common to all delays. The other coefficients are indexed since they include parameters related to the signal's driver and receiver.

Despite its simplicity, this Elmore-based modeling approach is widely used as a high-fidelity estimator in practical interconnect optimizations. Although it uses first-order capacitance approximations, and even though it does not account for signal slope effects, it is effective in guiding the search toward improved timing, as was verified by detailed circuit simulations on examples below. A multiplicative factor of 0.7 is generally used to fit the Elmore model with 50% signal delay. With more elaborate empirical parameter tuning, the model accuracy can be improved further: In [15], good absolute accuracy versus circuit simulation has been obtained by applying a parameter fitting procedure to a similar wire delay model, where the cross-capacitances were replaced by a fringing-field term.

IV. Sensitivity of Signal Delay-to–Wire Width and Spaces

Consider a single wire placed between two side-walls. The delay of the wire is given by (5), with $i = 1$. Partial derivatives with respect to W_1 and S_1 are as follows (note that the delay function is symmetrical in S variables $S_0 = S_1$):

$$\frac{\partial \Delta}{\partial W_1} = a_1 - \frac{1}{W_1^2}(c_1 + e) \tag{6}$$
$$\frac{\partial \Delta}{\partial S_1} = -\frac{1}{S_1^2}\left(d_1 + \frac{e}{W_1}\right). \tag{7}$$

Omitting the index $i = 1$, for each specific value of S the sensitivity to W is zero at a certain point $(W(\Delta_{\min}), S)$. This point is the minimum delay point for the given value of S. Sensitivity to S decreases monotonically with increasing of S and W.

In layout migration, wire width and spaces to neighbors cannot change independently. The additional constraint applied to W and S is

$$W + S_0 + S_1 = A, \text{ and therefore for fixed } S_1: \tag{8}$$
$$\frac{\partial \Delta}{\partial W} = -\frac{\partial \Delta}{\partial S_0}. \tag{9}$$

The sensitivities to both S and W are thus identical. An example is shown in Fig. 3 using 90-nm technology parameters for different driver resistances—100, 500, and 1000 Ω, driving

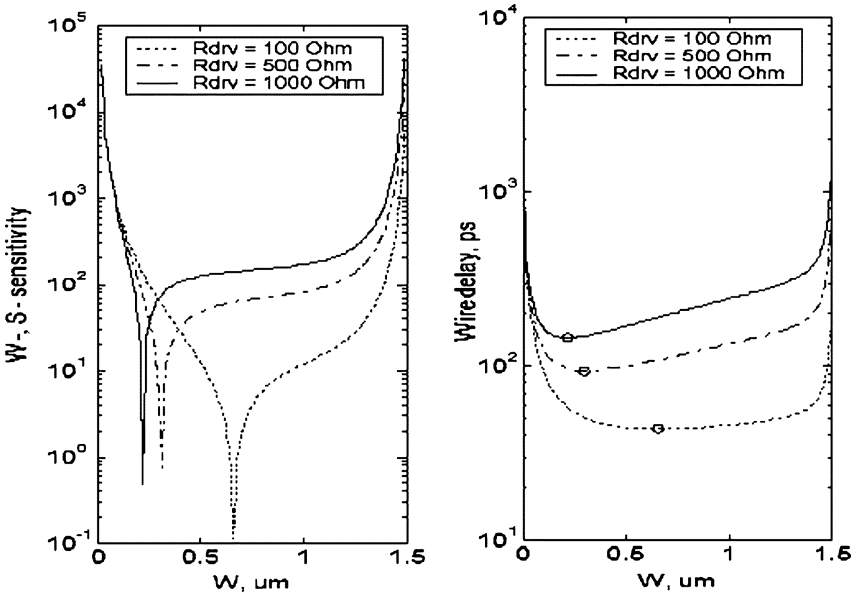


Fig. 3. Delay sensitivity to width and space for a single wire.

a wire of 1000-μm length, with load capacitance of 50 fF and the distance between walls is 1.5 μm. Sensitivity to both W and S was calculated for values of W from 0 to 1.5 μm. At the minimum delay point, sensitivity to wire width and spaces is zero, because the effect of any change in wire resistance balances out with the respective change in capacitances. A similar balance is obtained also when a bus with multiple wires is optimized, as will be discussed below. For wide buses, where inter-wire separation is large, the optimal width for each wire depends mostly on values of driver resistance and load capacitance of the wire, according to (8). This may be used as a first approximation for assigning initial values to wire widths in bus optimization.

V. Timing Objectives for Bus Optimization

We are seeking wire width and space allocation yielding "optimal timing." The definition of optimality depends on the design scenario. In the following we'll define four commonly used timing objectives.

First objective aims at maximizing the total sum of slacks (same as maximizing the average slack). Let T_i be the required time of the signal σ_i. The objective is thus defined as follows:

$$\begin{aligned} f_1(\overline{W},\overline{S}) &= \sum_{i=1}^{n} T_i - \Delta_i(\overline{W},\overline{S}) \\ &= \sum_{i=1}^{n} \left[T_i - \left(a_i W_i + b_i + \frac{c_i}{W_i} + \left(d_i + \frac{e}{W_i} \right) \right.\right. \\ &\qquad \left.\left. \times \left(\frac{1}{S_{i-1}} + \frac{1}{S_i} \right) \right) \right]. \end{aligned} \tag{10}$$

When required times are still undetermined, an objective of minimizing total sum of delays is commonly used. Notice that from a mathematical point of view this is equivalent to maximizing the first objective, since

$$f_2(\overline{W},\overline{S}) = \sum_{i=1}^{n} \Delta_i(\overline{W},\overline{S}) = -f_1(\overline{W},\overline{S}) + \sum_{i=1}^{n} T_i. \tag{11}$$

The term $\sum_{i=1}^{n} T_i$ however is constant and does not affect the optimization. In the sequel we'll discuss the minimization of total sum of delays f_2. Without loss of generality the results are applicable to maximization of total slack f_1.

Both (10) and (11) are cumulative metrics, integrating the contribution of all signal wires. These are useful objectives for design migration, where the goal is to deliver overall timing speedup. The important factor in such a design scenario is the average speedup, which is well reflected by (10) and (11).

When tuning of critical signals is of interest, the design scenario calls for *MinMax* optimization problems. Hence, a third objective is to minimize the worst slack among all signals, expressed by f_3 below. Note that we exchanged the terms of the slack for the sake of mathematical convenience

$$f_3(\overline{W},\overline{S}) = \max_{1\le i\le n} \left\{ \Delta_i(\overline{W},\overline{S}) - T_i \right\}. \tag{12}$$

A fourth objective aims at minimizing the delay of the slowest signal in the bus. It can be used when timing constraints are not known yet. The corresponding objective function is

$$f_4(\overline{W},\overline{S}) = \max_{1\le i\le n} \left\{ \Delta_i(\overline{W},\overline{S}) \right\}. \tag{13}$$

In the following, we will explore the optimization of the objective functions f_1 through f_4 by varying the widths and spaces of the bus wires. We first note that all the objectives have a global optimum since the underlying problems are all convex or concave. The convexity proof is given in Appendix A. Additional useful properties of the underlying optimization that suggest efficient solutions are discussed below. Let us ignore design rules (2) and (3) for the sake of easing the analysis. These do not change the nature of the problem.

VI. Optimizing Total Sum of Slacks or Delays

We are aiming at minimizing (11) subject to (1). In order to find the minimum of f_2 under g constraint, let us calculate partial derivatives

$$\frac{\partial f_2}{\partial W_i} = a_i - \frac{c_i}{W_i^2} - \frac{e}{W_i^2}\left(\frac{1}{S_{i-1}} + \frac{1}{S_i}\right) \quad i = 1, \ldots, n \tag{14}$$

$$\frac{\partial f_2}{\partial S_i} = -\frac{1}{S_i^2}\left[d_i + d_{i+1} + e\left(\frac{1}{W_{i+1}} + \frac{1}{W_i}\right)\right], \quad i = 0, \ldots, n \tag{15}$$

$$\frac{\partial g}{\partial W_i} = 1, \qquad 1 \le i \le n \tag{16}$$

$$\frac{\partial g}{\partial S_i} = 1, \qquad 0 \le i \le n. \tag{17}$$

At minimum, there exists some real number λ (Lagrange multiplier), satisfying $\nabla f_1 = \lambda \nabla g$. Rearranging and substituting yields the following:

$$\lambda = a_i - \frac{1}{W_i^2}\left[c_i + e\left(\frac{1}{S_{i-1}} + \frac{1}{S_i}\right)\right], \quad i = 1, \ldots, n \tag{18}$$

$$\lambda = -\frac{1}{S_i^2}\left[d_i + d_{i+1} + e\left(\frac{1}{W_{i+1}} + \frac{1}{W_i}\right)\right], \quad i = 0, \ldots, n. \tag{19}$$

We define $W_0 = W_{n+1} = \infty$ to represent a sidewall connected to power or ground. The above equations plus the area constraint equation (1) impose $2n + 2$ algebraic equations in $2n + 2$ variables λ, $W_1 \cdots W_n$, $S_0 \cdots S_n$.

The equations to obtain the maximum of total sum of slacks are identical to (18) and (19). Similar arguments hold, except that minimum is replaced by maximum and convexity by concavity.

VII. Minimizing Maximal Delays and Negative Slack: MinMax Problems

Objective functions (12) and (13) dealing with worst delay and slack are not differentiable. Therefore, the respective MinMax optimization problems cannot be solved analytically. Although general convex programming or Lagrange relaxation [7] can be employed, we propose a solution approach based on the following properties of these specific problems, yielding an efficient iterative solution with guaranteed convergence.

Theorem 1 (Necessary Condition): In the optimal solution of minimizing the maximal delay in (13) [worst slack in (12)] subject to the area constraint (1), all the delays (slacks) are equal.

Proof: Let us prove the case of delays. Assume on the contrary that the above assertion does not hold. Namely, in the optimal solution, there exists a wire i whose associated delay is greater than all others. If there are few maximal ones, pick one having a neighbor with a smaller delay. Such one must exist, as otherwise the delays satisfy the statement of the theorem.

There exist therefore signals σ_{i-1}, σ_i and σ_{i+1}, such that their corresponding delays Δ_{i-1}, Δ_i and Δ_{i+1}, respectively, satisfy $\Delta_{i-1} < \Delta_i$ and $\Delta_{i+1} \le \Delta_i$. We may now narrow wire $i - 1$ slightly, thus increasing its delay, say by a magnitude that does not exceed $(\Delta_i - \Delta_{i-1})/2$ in the worst case. We may similarly narrow wire $i + 1$ and increase its delay by $(\Delta_i - \Delta_{i+1})2$ if $\Delta_{i+1} < \Delta_i$ indeed. Such narrowing must reduce Δ_i since the width of wire i didn't change, but its spacing from neighbors was increased. Δ_i Which was a maximal delay was thus reduced. If this was the single maximal delay, a contradiction follows since the maximal delay was reduced, while other delays do not exceed it. If there are several wires with maximal delay, the same procedure repeats itself for the next maximal delay wire, until all maximal delays are reduced. This procedure must terminate since the problem it finite.

The proof for objective of worst negative slack follows similarly. •

Theorem 1 imposes necessary conditions on optimal solutions. It is not true that any solution whose delays (or slacks) are all equal is optimal. The convexity of the max objective functions ensures a unique and global minimum. These functions are continuous but not differentiable, so we cannot rely on equating first derivatives to zero in order to express sufficient conditions for optimality. We'll instead attempt to change one of the space or width variables. A single variable however cannot change alone due to the area constraint. We'll therefore attempt to make a local change of a triplet (S_{i-1}, W_i, S_i) or (W_i, S_i, W_{i+1}), without changing any other variable, such that $S_{i-1} + W_i + S_i$ or $W_i + S_i + W_{i+1}$ are invariant. We define this as an *area preserving local modification*. Clearly, it affects only the delays of $(\sigma_{i-1}, \sigma_i, \sigma_{i+1})$ or (σ_i, σ_{i+1}), respectively. All other delays are unaffected.[1]

Let $\varepsilon > 0$ be arbitrarily small and $0 \le \alpha \le 1$ be real positive numbers. Area preserving local modification of (S_{i-1}, W_i, S_i) will result in the triplet $(S_{i-1} \mp \alpha\varepsilon, W_i \pm \varepsilon, S_i \mp (1-\alpha)\varepsilon)$, for which wire width is increased (decreased), while its neighbor spaces are decreased (increased). Similarly, the modification of (W_i, S_i, W_{i+1}) will result in the triplet $(W_i \mp \alpha\varepsilon, S_i \pm \varepsilon, W_{i+1} \mp (1-\alpha)\varepsilon)$. Notice the correspondence between the plus and minus signs in the modified triplets.

Since max delay (or worst slack) is a convex objective whose global minimum is the MinMax point, the following statement is in order.

Postulate: For any equal delay (or slack) solution other than the MinMax one, there exists an area preserving local modification which reduces the delay (or slack) of a signal without increasing the delay of any other signal.

The following theorem provides a sufficient condition for an equal delay (or slack) solution to be the global minimum.

Theorem 2 (Sufficient Condition): Let all the delays in max delay (worst slack) objective function be equal to each other. This is then the MinMax solution if for all i and any $0 \le \alpha \le 1$ the following relations exist:

$$a_i - \frac{c_i}{W_i^2} + \left(d_i + \frac{e}{W_i}\right)\left(\frac{\alpha}{S_{i-1}^2} + \frac{1-\alpha}{S_i^2}\right) - \frac{e}{W_i^2}\left(\frac{1}{S_{i-1}} + \frac{1}{S_i}\right) = 0 \tag{20}$$

[1]This is true under the assumptions stated in this paper, because signal slope effects are neglected. However, in reality cross-coupling might slightly affect other delays, as a result of slope change.

$$\left[-a_i + \frac{c_i}{W_i^2} + \frac{e}{W_i^2}\left(\frac{1}{S_{i-1}} + \frac{1}{S_i}\right)\right] - \left(d_i + \frac{e}{W_i}\right)\frac{1}{S_i^2} = 0 \quad (21)$$

$$\left[-a_{i+1} + \frac{c_{i+1}}{W_{i+1}^2} + \frac{e}{W_{i+1}^2}\left(\frac{1}{S_i} + \frac{1}{S_{i+1}}\right)\right] - \left(d_{i+1} + \frac{e}{W_{i+1}}\right)\frac{1}{S_i^2} = 0 \quad (22)$$

where a_i, c_i, d_i, and e are the coefficient of delay (5). The proof can be found in Appendix C. Notice that the terms comprising the conditions (20), (22) are reminiscent of the derivatives in (14) and (15). Hence, an equal delay (slack) solution is optimal if no area-preserving local modification can be found to improve any of the bus wires.

VIII. Iterative Algorithm for MinMax Delay or Slack

Theorems 1 and 2, and the convexity properties discussed earlier suggest an iterative algorithm to obtain a minimum of maximal delay (It can be easily adapted to maximize the most critical slack). The algorithm works in two phases which repeat themselves until convergence.

The first phase equates the delay of all signals by iterations. It picks the signal whose delay is currently maximal. It then reduces the delay by equating it with its two neighbors, a technique used in the proof of Theorem 1. This is repeated until all delays are equal.

The second phase checks for existence of the sufficient condition posted in Theorem 2. It then picks the triplet which mostly violates the sufficient condition and performs an optimal area preserving local modification which is reducing the delay of the triplet's signals.

This gives a rise for another iteration of first phase, as the delay of all the signals can equate at a lower value. If the sufficient condition is satisfied however, the algorithm terminates at optimum.

The algorithm for maximal delay minimization is outlined below. Some heuristics aiming at speeding up convergence are included.

```
MinMaxDelay ()
set initial solution;
do {
  while (not all signal delays are
equal) {// first phase
    1. Pick signal with maximal delay;
    2. Equate delay of the selected
signal with its two neighbors
  }
if (sufficient condition fulfilled)
    terminate; // optimum reached
  else // second phase
    1. Find the triplet which vio-
lates the sufficient condition most
strongly;
    2. Reduce delay of triplet's signal
by area preserving local modification;
}
```

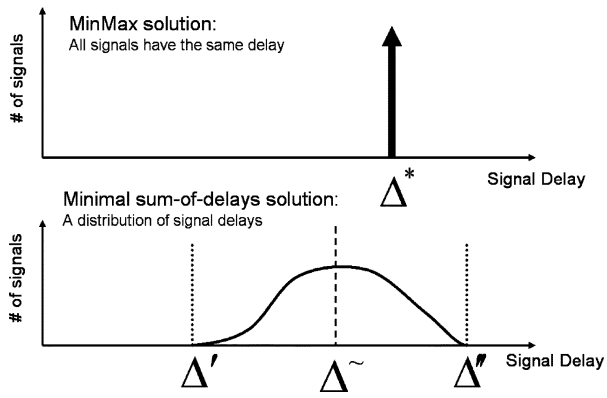


Fig. 4. Distributions of signal delays in MinMax solution (top) compared with minimal sum-of-delays solution (bottom).

Convergence of the above algorithm can be proven as follows: The inner loop of ***while*** (first phase) iterates over signals and reduces the maximal delay. Therefore, the maximal delay, which is positive, is monotonically decreasing. Hence, it must reach a limit. In the outer ***do*** loop the delay (equal for all signals) is also monotonically decreasing, thus it must reach a limit as well.

IX. Relation Between Minimal Total Sum and MinMax Solutions

We further study the relation between the optimal solutions of total sum and MinMax optimizations, for either delay or slack optimizations. We may interpret the delay (slack) of the bus $\Delta \equiv (\Delta_1, \ldots, \Delta_n)$ (analogously for slacks) as a vector in n-dimensional vector space over real positive numbers. The addition of delay (slack) vectors is interpreted as connecting two busses serially, signal by signal. It is not difficult to prove that the objective function of total sum of slacks (10) or delays (11), and the objective function of max slack (12) or delay (13) are nothing but the norms $\| \|_1$ and $\| \|_\infty$, respectively. Let $v \in V$ be any vector in n-dimensional vector space V. The *norm equivalence theorem* states that there exist real positive numbers α and β satisfying $\alpha < \|v\|_1/\|v\|_\infty < \beta$. This means that an optimal solution of minimizing the total sum of delays is also a good MinMax solution and vice versa. Indeed, the following theorems claim that the optimal solution of the MinMax problem is bounded from both sides by the optimal solution of the total sum problem. The notation is shown in Fig. 4, illustrating distributions of signal delays in the solution of a minimal total delay problem and in the solution of the corresponding MinMax delay problem.

Theorem 3: Let Δ', $\Delta^\sim$ and Δ'' be the smallest, average and largest delay, respectively, among all the bus signals in the optimal solution of minimal total sum of delay. Let Δ^* be the delay of each signal in the MinMax optimal solution. There exists then $\Delta' \le \Delta^\sim \le \Delta^* \le \Delta''$.

Proof: The inequality $\Delta' \le \Delta^\sim \le \Delta''$ is satisfied by definition. It is impossible that $\Delta^* < \Delta^\sim$. Otherwise, the optimal MinMax solution yields total sum of delay $n\Delta^*$, thus contradicting the optimality of $n\Delta^\sim$. It is also impossible that $\Delta'' < \Delta^*$ as it yields a solution whose max delay is smaller than Δ^*, contradicting the optimality of Δ^*. •

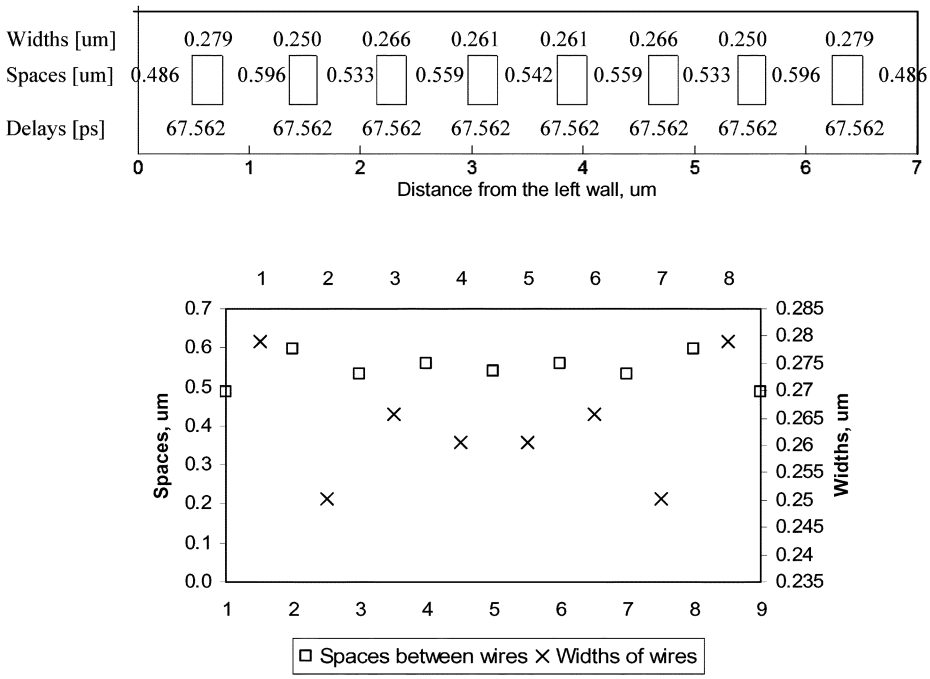


Fig. 5. (Top): cross section of the bus after MinMax delay optimization, annotated with values of wire widths and spaces. (Bottom): width and spaces shown as graphs versus wire position in the bus.

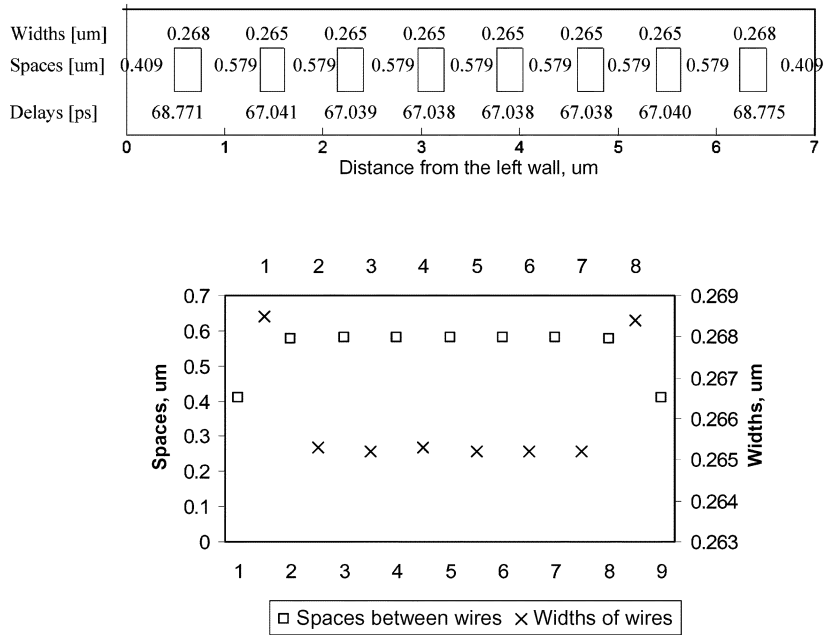


Fig. 6. (Top): cross section of the bus after sum-of-delays optimization, annotated with values of wire widths and spaces. (Bottom): width and spaces shown as graphs versus wire position in the bus.

Theorem 4: Let Ω', $\Omega^{\sim}$ and Ω'' be the smallest, average and largest slack of a signal, respectively, in the optimal solution of maximal total sum of slack. Let Ω^* be the slack of a signal in the MinMax optimal solution. There exists then $\Omega' \leq \Omega^{\sim} \leq \Omega^* \leq \Omega''$.

X. Examples

Exampel 1: Sidewall Effects in a Uniform Bus: Figs. 5 and 6 illustrate the optimal solutions of MinMax and sum-of-delays optimization, respectively. The bus has eight signals whose wire length is 500 μm. All drivers are of 500-Ω resistance and all load capacitances are 50 fF. The area allocated for the bus is 7 μm.

In case of MinMax optimization all signal delays are identical as expected. Notice that wire width and space have "oscillations" decaying toward the center of the bus. This is caused by the side walls, which get relatively small spaces to the extreme wires, because unlike all other spaces their cross-capacitance is not shared by two signals. The narrow space needs compensa-

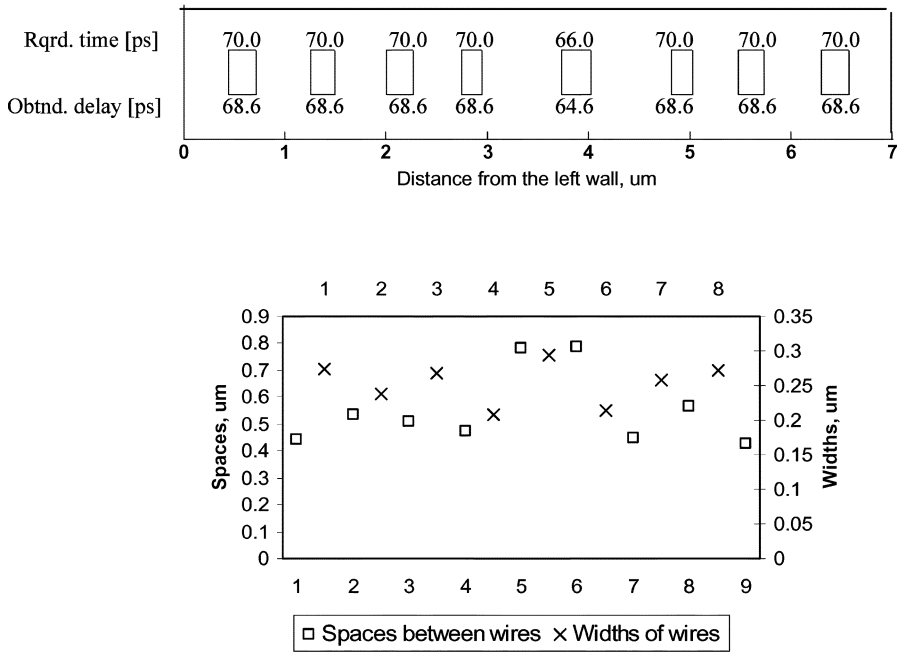


Fig. 7. (Top): cross section of the bus after MinMax slack optimization. (Bottom): width and spaces shown as graphs versus wire position in the bus.

tion by a wide wire, otherwise large RC delay will occur. This phenomenon repeats itself for the next adjacent wires, with decreasing amplitude. In the minimization of sum-of-delays, the first and last wires are affected similarly as in MinMax optimization due to same reason: sidewalls don't care for space. All other signals however have the same width and space. Consequently, the extreme wires have larger delay than all others. Despite differences in width-space distributions between two cases, numerical values of delays are very close. Comparing average delay obtained in sum-of-delays optimization with delay obtained by MinMax optimization yield $\Delta^{\sim} = 67.473$ ps and $\Delta^* = 67.562$ ps, which are indeed very close.

For deeper insight while comparing total sum-of-delays with MinMax problems, let's simplify the bus model and ignore the sidewall effect. This is done by dropping the sidewalls and assuming that the leftmost signal and the rightmost signal are adjacent. Pictorially, it is equivalent to placing the signal bus on a cylindrical surface, thus obtaining two neighbors for every signal. The optimal solution satisfies the following theorem whose proof is given in Appendix B.

Theorem 5: Let all signals have identical drivers and identical receivers and let their order be cyclical (placed on a cylindrical surface). Then in the optimal solution of maximizing (minimizing) the total sum of slacks (delays), all the widths, spaces and delays are necessarily equal.

We now characterize the optimal solution of MinMax delay in a cyclical uniform bus by a direct consequence of Theorems 3 and 5 above.

Corollary 1: For a cyclical bus where all signals have identical drivers and identical receivers, the minimization of max delay yields the same solution as the minimization of total sum of delays.

Proof: Follows directly from Theorem 3 which states that $\Delta' \leq \Delta^{\sim} \leq \Delta^* \leq \Delta''$, where Δ', $\Delta^{\sim}$ and Δ'' are the smallest, average and largest delays in the minimal total sum of delays, respectively, and Δ^* is the delay of a signal in the optimal MinMax solution. Theorem 5 states that for cyclic uniform bus there exists $\Delta' = \Delta^{\sim} = \Delta''$. Hence, the corollary follows. •

Returning to Example 1 above, let us modify the bus to be cyclical. Both MinMax optimization and minimal sum-of-delay optimization were solved in MATLAB and yielded a result 65.524 ps. In conclusion, a uniform bus is similar to a cyclical bus, except for the edge effects near the sidewalls. Therefore, optimal solutions for total delay and MinMax delay are almost identical. Note that the identity of optimal solutions for total sum and MinMax does not exist for slacks, even in a uniform cyclical bus. Maximizing total sum of slacks is the same as minimizing total sum of delays; hence delays of signals are all equal in the optimized uniform cyclical bus. Slacks, however, are not equal to each other as they depend on the required time which may change from signal to signal. In the optimal solution of the MinMax slack problem, all slacks are equal.

The next example deals with optimizing total slack and worst slack in a uniform bus with side walls.

Example 2: Slack Optimization: Fig. 7 illustrates the case where a required time is assigned to each signal. Using the same bus from Example 1, a required time of 65 picoseconds was assigned to the fifth wire, while all other wires were allowed 70 picoseconds. Applying MinMax optimization of the slacks results in equal slacks of 1.4 picoseconds for all signals, as shown in Fig. 7. The distribution of wire widths and spaces is depicted in the bottom part of Fig. 7. Its nature is similar to the case of MinMax delay optimization. Notice however that the nonuniformity in required time disturbs the symmetry obtained in Example 1.

The wire which was assigned the most difficult (earliest) required time became wide, while its spacing to adjacent wires became larger too. This is for the sake of reducing its *RC* delay, thus compensating for the early required time.

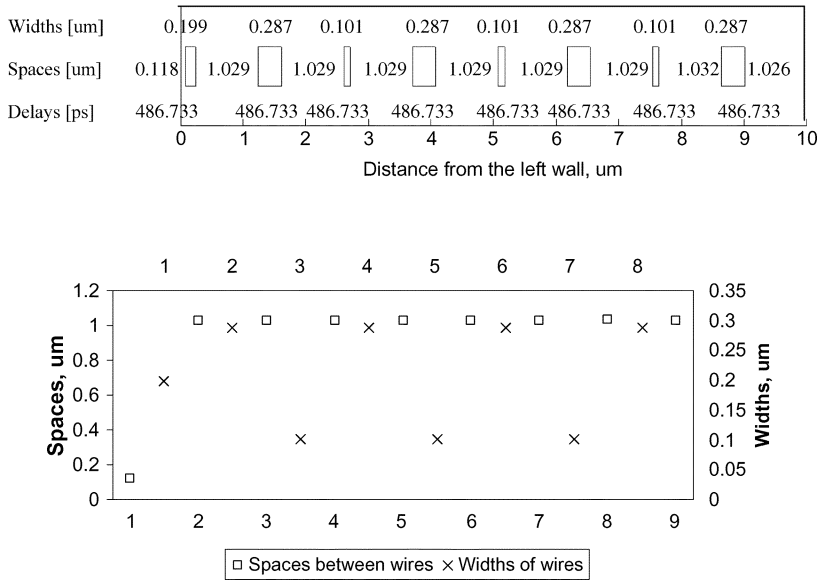
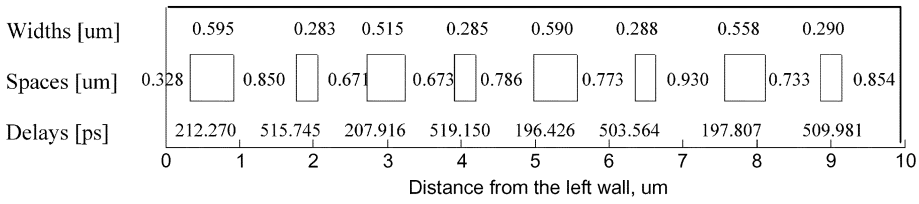


Fig. 8. Nonuniform bus minmax optimization.



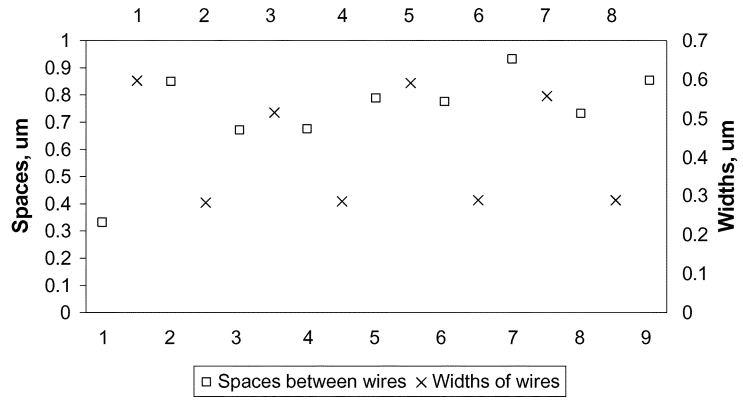


Fig. 9. Nonuniform bus total sum of delays optimization.

Recall that maximizing total sum of slack is not affected by required times as this optimization is identical to minimizing total delay, as discussed earlier.

Example 3: Non-Uniform Bus: This example presents an interleaved bus structure, with alternating drivers; odd-numbered wires have strong drivers $(R_d = 100\ \Omega)$, and even-numbered wires have weak drivers $(R_d = 1000\ \Omega)$. Wire length is 3000 μm and load capacitance 70 fF in this example. A total bus width is constrained to 10 μm. Results of optimizing this bus are depicted in Figs. 8 and 9. Notice first that the wire width and space distributions of MinMax optimization differ significantly from total sum-of-delays minimization. Since in MinMax optimization all the delays must be equal, and since the weak and strong drivers are interleaved, the spaces must be equal to each other. An exception is the leftmost space. This is due to the asymmetry resulting from a strong driver on the left side and a weak driver on the right side of the bus. The equality of spaces and signal delays implies that signals with strong drivers will be narrower than those driven by weak drivers, as demonstrated in the bus cross section. Minimization of total sum-of-delay also yields alternating widths of wires, but neither uniformity nor symmetry exists. Notice also that wider wires were allocated to strong drivers in this case. It is interesting to compare the delays obtained by the two optimizations. Although all the relations proved in Theorem 3 do exist, the MinMax delay is much worse than the average delay in the total sum-of-delay optimization. In fact, it is very close to the maximal delay of the latter distribution.

TABLE I
MIGRATION OF CIRCUIT BLOCK IN 65 NANOMETER TECHNOLOGY

Wire no.(i)	R_{driver} [$K\Omega$]	C_{load} [fF]	Before optimization			After optimization		
			S_{i-1} [μm]	W_i [μm]	Delay (% of clock cycle time)	S_{i-1} [μm]	W_i [μm]	Delay (% of clock cycle time)
1	2.17	0.75	0.33	0.33	46.5	0.54	0.11	34.9
2	2.17	0.75	0.33	0.33	44.5	0.86	0.11	33.2
3	0.085	14	0.33	0.33	6.4	0.46	0.11	14.3
4	2.17	0.75	0.33	0.33	44.8	0.65	0.11	32.9
5	0.085	14	0.33	0.33	6.4	0.72	0.11	10.8
6	2.17	0.75	0.33	0.33	45.2	0.29	0.11	38.3
7	0.085	14	0.33	0.33	6.4	0.26	0.16	10.3
8	2.17	0.75	0.33	0.33	44.0	0.34	0.11	36.0
9	2.17	0.75	0.33	0.33	44.2	0.31	0.11	34.4
10	2.17	0.75	0.33	0.33	43.8	0.7	0.11	32.6
11	0.085	14	0.33	0.33	6.6	0.47	0.14	13.0
12	0.085	14	0.33	0.33	6.2	0.21	0.11	14.8
13	2.17	0.75	0.33	0.33	44.1	0.9	0.11	32.4
14	2.17	0.75	0.33	0.33	44.1	0.58	0.11	33.4
15	0.085	14	0.33	0.33	6.6	0.42	0.11	14.6
16	2.17	0.75	0.33	0.33	44.6	0.42	0.11	33.4
17	0.085	14	0.33	0.33	6.6	0.93	0.16	9.7
18	2.17	0.75	0.33	0.33	45.2	0.52	0.11	34.2
19	0.085	14	0.33	0.33	6.6	0.5	0.11	14.7
20	2.17	0.75	0.33	0.33	44.6	0.57	0.11	33.4
Average					**29.4**			**25.6**

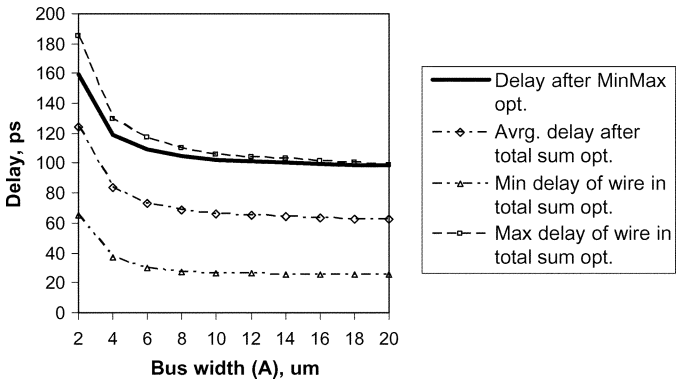


Fig. 10. Optimal solution parameters Δ', $\Delta^{\sim}$, Δ^{*}, Δ'' (see Fig. 4) versus bus width constraint A, for the circuit of Example 4.

Example 5: Optimal Delay Dependency on Bus Width: Let us change the total width of the bus in Example 4. The MinMax delay is compared to the minimum, average and maximum delay of the corresponding total sum-of-delays optimization, for various bus widths, as illustrated in Fig. 10. According to Theorem 3, the MinMax delay of all wires always resides between the average and the maximal wire delay in the total sum-of-delay minimization. As the bus width constraint is relaxed (larger widths), the MinMax result approaches the maximal delay of the other optimization. This is due to the fact that large bus width decouples the signals, so signals of weak and strong drivers are optimized independently.

Example 6. Migration of a Bus in an Industrial Circuit: A 20-wire metal 3-bus structure from an industrial circuit block was migrated from 90- to 65-nm technology, with a clock frequency target of several GHz. The total width of the bus is 13.53 μm, length of wires is 500μm. Before optimization, wire widths and spaces were determined by shrinking the old layout, as specified in Table I below. Two kinds of drivers are used in the bus: strong drivers with resistance of 85 Ω and input capacitance of 14 fF and weak drivers with resistance of 2.17 kΩ put capacitance of 0.75 fF.

Total sum of delays timing optimization was run on this bus and results are presented in Table I. The delays in Table I were obtained from circuit simulations, performed with extracted parasitics from actual layouts before and after optimization, using accurate industrial tools. The delays are represented as a percentage of the clock cycle time. As seen in the table, average timing of the bus was improved by about 13%. It was achieved by decreasing widths of wires and varying spaces, thus decreasing wire capacitances on the slower signals. As expected, the timing improvement of critical signals as well as the improvement in total sum of delays were obtained by trading off the less critical signals whose delay got worse. Almost all wires were narrowed to the minimal allowed value of 0.11 μm. Since the bus is relatively short, wire resistance effect is not critical and therefore most of the channel area was allocated to inter wire spaces in order to decrease loading of weak drivers by inter-wire cross capacitances. Minimization of worst wire

delay has also been performed, and results were verified by circuit simulation, using extracted layout capacitances and resistances, yielding 36.2% of clock cycle time versus 46.5% before optimization (compare with the average wire delay of 25.6% and maximum wire delay of 38.3% in sum of delays optimization). Elmore delay estimates were about 35% larger than circuit simulation results.

XI. Discussion and Conclusion

It has been noted in general circuit timing optimization that whenever MinMax formulation is used, all timing paths tend to become equally critical, as proven in theorem 1 for the bus sizing problem. This phenomenon was termed path-balancing [17], [18]. Shaping of delay distributions involves a number of considerations: minimization of critical delay for maximal circuit speed tends to push the right tail of the path delay distribution toward the center, and minimization of area and power often tends to push the left tail toward the center. Circuit tuning by MinMax optimization results in a very narrow distribution of delays, as illustrated in Fig. 4. However, a narrow distribution where many paths are critical, is more sensitive to parameter variability [17]–[19]. A modification of the objective function in MinMax formulation has been proposed, involving a penalty function [18] which separates the most critical paths from others. An alternative approach is to use the total sum objective, at least in the initial stages of layout migration. At the optimal the solution of total sum minimization, every wire is at a balance point where sensitivity to the value of wire width and spaces approaches zero, as illustrated in Fig. 3. In contrast, the MinMax solution takes most signals away from this stable point in order to equalize all of the delays or slacks, and therefore the circuit becomes more sensitive to variations in geometrical dimensions. Our computational experiments in bus tuning show that typically, most signal delays become much worse while the critical signal become only slightly better as resources are shifted to make all wires equally critical. In other words, the largest wire delay in the total sum solution is typically a tight bound on the solution of the MinMax problem, as seen in the example of Fig. 9.

In conclusion, we have characterized the problem of simultaneously allocating wire widths and spaces to all wires in parallel bus structures under a total area constraint, for circuit performance optimization. We have demonstrated its importance in migration of layouts to new generations of CMOS process technology. Our results show that total sum of delays (or slacks) is a useful objective function for minimization. Compared with MinMax delay tuning, it is mathematically more convenient, leads to robust solutions which are less sensitive to parameter variations, and typically produces bus layouts which closely approach the best achievable performance. We have also presented an iterative algorithm for MinMax performance tuning of bus layouts, based on problem-specific necessary and sufficient conditions for optimality.

Appendix A
The Optimization Problems are All Convex

Proposition: The objectives functions f_1, f_2, f_3, f_4 presented above are all convex or concave. Their associated constraints are linear, and therefore also convex. Consequently all the optimization problems have unique, global minimum or maximum, depending on convexity or concavity.

Proof: The area and design rules constraints given in (3), (4) and (5) are all linear equalities or inequalities. Altogether they define a convex feasible region on which the above objective functions are defined.

The function $\Delta_i(\overline{W},\overline{S})$ in (2) is a sum of terms depending on the variables W_i, S_i and S_{i-1}. In order to prove its convexity it is sufficient to see the convexity for each term, since a linear combination with positive coefficients of convex functions is convex too. Convexity exists if all its second order derivatives are nonnegative. Deriving twice all the terms comprising Δ yields $\partial W/\partial^2 = 0$; $(\partial 1/W)/\partial^2 W = 2/W^3 > 0$; $(\partial 1/WS)/\partial^2 W = 2/W^3 S > 0$; $(\partial 1/WS)/\partial W \partial S = (\partial 1/WS)/\partial S \partial W = 1/W^2 S^2 > 0$; $(\partial 1/WS)/\partial^2 S = 2/WS^3 > 0$, which are all nonnegative. Consequently, the delay of single signal is convex

The function f_1 defined in (10) is a negative sum of convex terms and therefore yields a concave function. Its maximization on convex region yields unique global maximum. For similar reasons, f_2 defined in (11) is convex and has therefore global minimum.

Both functions f_3 and f_4 of maximal slack delay as defined in (12) and (13), respectively, are convex since they are a maximum of convex functions. Their minimization on convex region yields therefore a unique global minimum. •

Appendix B
Proof of Theorem 5

Proof: From (11) we obtain

$$f_2 = a\sum_{i=1}^{n} W_i + nb + c\sum_{i=1}^{n}\frac{1}{W_i} + 2d\sum_{i=1}^{n}\frac{1}{S_i} + e\left[\sum_{i=2}^{n}\frac{1}{W_i}\left(\frac{1}{S_{i-1}}+\frac{1}{S_i}\right)+\frac{1}{W_1}\left(\frac{1}{S_n}+\frac{1}{S_1}\right)\right]. \quad (23)$$

In the above, we identify S_0 with S_n due to the cyclic ordering of signals. Note also that the coefficients are not indexed since all drivers and receivers are identical.

Assume that the optimization problem (3), (18) and (19) was solved and the optimal solution is given. Let $W = \sum_{j=1}^{n} W_j$ and $S = \sum_{j=1}^{n} S_j$ denote the total wire widths and total spacing in the optimal solution. Obviously, there exists $A = W + S$. Let us show that among all the settings of area preserving W and s, the one in which all W_i and S_i are identical is optimal.

Examination of (23) shows that it consists of the following sums $\sum_{i=1}^{n} 1/W_i$, $\sum_{i=1}^{n} 1/S_i$ and $t(\overline{W},\overline{S}) = \sum_{i=2}^{n}[1/W_i(1/S_{i-1} + 1/S_i] + 1/W_1(1/S_n + 1/S_1)$. The first two sums are minimized only when all W_i are equalized and all S_i are equalized. We'll show the term $t(\overline{W},\overline{S})$ is also minimized by such equalization.

Substitution of $W_n = W - \sum_{j=1}^{n-1} W_j$ and $S_n = S - \sum_{j=1}^{n-1} S_j$ in $t(\overline{W},\overline{S})$ and then differentiating by each of the

$2n-2$ variables $W_1,\ldots,W_{n-1},S_1,\ldots,S_{n-1}$ yields

$$\frac{\partial t}{\partial W_i}=\frac{1}{W_i^2}\left(\frac{1}{S_{i-1}}+\frac{1}{S_i}\right)+\frac{1}{\left(W-\sum_{j=1}^{n-1}W_j\right)^2}\times\left(\frac{1}{S_1}+\frac{1}{S-\sum_{j=1}^{n-1}S_j}\right)=0 \tag{24}$$

$$\frac{\partial t}{\partial S_i}=\frac{1}{S_i^2}\left(\frac{1}{W_i}+\frac{1}{W_{i+1}}\right)+\frac{1}{\left(S-\sum_{j=1}^{n-1}S_j\right)^2}\times\left(\frac{1}{W_{n-1}}+\frac{1}{W-\sum_{j=1}^{n-1}W_j}\right)=0. \tag{25}$$

Note that in both (24) and (25) the second term is identical and independent of i for all equations. Consequently, all the derivatives of $t(\overline{W},\overline{S})$ by widths satisfy same equation, and so the derivatives by spacing. Therefore, there exist two real numbers λ_w and λ_s, satisfying $1/W_i^2(1/S_{i-1}+1/S_i)=\lambda_w$ and $1/S_i^2(1/W_i+1/W_{i+1})=\lambda_s$. This implies that $W_1=W_2=\ldots=W_n$ and $S_1=S_2=\ldots=S_n$ is indeed the optimal and unique solution.

In conclusion, minimal total sum of delays requires identical wire widths and identical wire spacing. Identical signal delays follow immediately due to identical drivers and identical receivers. •

Appendix C
Proof of Theorem 2

Proof: Assume to the contrary that a given equal delay solution is not minimal. According to the above postulate there exists area preserving local modifications that will reduce the delay of a signal without increasing the delay of any other signal. Four modifications are possible: Increasing or decreasing wire width, and increasing or decreasing a space. Let us consider each.

Case 1) Increasing wire width is impossible since area preservation implies that at least one of the adjacent spaces is decreased. This however increases the delay of the adjacent signal that shares this space.

Case 2) Decreasing the width results in the new triplet $(S_{i-1}+\alpha\varepsilon,W_i-\varepsilon,S_i+(1-\alpha)\varepsilon)$, where $0\le\alpha\le 1$. The delays Δ_{i-1} and Δ_{i+1} do not increase as their adjacent spaces do decrease. For the new delay Δ_i' to decrease there must exist some $0\le\alpha\le 1$, such that substitution of the new width and spaces in (2) yields

$$0\le\Delta_i-\Delta_i'=\varepsilon\left[a_i-\frac{c_i}{W_i^2}+\left(d_i+\frac{e}{W_i}\right)\left(\frac{\alpha}{S_{i-1}^2}+\frac{1-\alpha}{S_i^2}\right)-\frac{e}{W_i^2}\left(\frac{1}{S_{i-1}}+\frac{1}{S_i}\right)\right]+O(\varepsilon^2)$$

Dropping the term $O(\varepsilon^2)$ implies that delay reduction requires the above square brackets to be positive. Case 1 can be viewed as being obtained by using negative ε, thus implying an opposite inequality than the above. Hence, (20) follows.

Case 3) Decreasing a space results in the new triplet $(W_i+\alpha\varepsilon,S_i-\varepsilon,W_{i+1}+(1-\alpha)\varepsilon)$. We require that none of Δ_i and Δ_{i+1} is increased. This implies the for some $0\le\alpha\le 1$, there exists

$$0\le\Delta_i-\Delta_i'=\varepsilon\left\{\alpha\left[-a_i+\frac{c_i}{W_i^2}+\frac{e}{W_i^2}\left(\frac{1}{S_{i-1}}+\frac{1}{S_i}\right)\right]-\left(d_i+\frac{e}{W_i}\right)\frac{1}{S_i^2}\right\}+O(\varepsilon^2)$$

$$0\le\Delta_{i+1}-\Delta_{i+1}'=\varepsilon\left\{(1-\alpha)\left[-a_{i+1}+\frac{c_i}{W_{i+1}^2}+\frac{e}{W_{i+1}^2}\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right)\right]-\left(d_{i+1}+\frac{e}{W_{i+1}}\right)\frac{1}{S_i^2}\right\}+O(\varepsilon^2)$$

Dropping the term $O(\varepsilon^2)$ implies that delay reduction requires the above square brackets to be positive. Hence, (21) and (22) must be non-negative.

Case 4) Increasing a space results in the new triplet $(W_i-\alpha\varepsilon,S_i+\varepsilon,W_{i+1}-(1-\alpha)\varepsilon)$. This is exactly the same as case 3, but with negative ε. Therefore, the braces need now be non-positive. •

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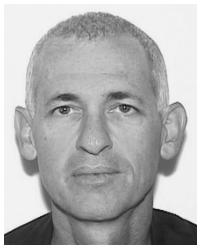

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