BAR-ILAN UNIVERSITY (RA)

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אוניברסיטת בר-אילן (ע"ר)

בית הספר להנדסה

רמת-גן 52900

27 מרץ 2012 **פרופ' שמואל וימר**

מבוא לתכנון מעגלי VLSI

תשע"ב סמס' א' מועד ב'

- יש לענות על כל השאלות. משקל השאלות השונות נתון בגוף השאלות.
- **יש לנמק את כל תשובותיכם**. אין צורך לפתח מחדש תוצאות שהוכחו בכיתה, אלא אם כן נאמר מפורשות לעשות כן.
- משך המבחן שלש שעות.
- יש לשרטט מערכות ודיאגראמות באופן ברור ! הכתיבה בעט בלבד. כתיבה בעפרון לא תבדק!
- סך כל הנקודות הוא 120, הציון המירבי בכל מקרה לא יעלה על 100.
- השמוש בכל חומר כתוב (ספרים, רשימות) מותר .השמוש במחשב או בכל אמצעי אלקטרוני אחר אסור בהחלט.

בהצלחה

Problem No 1 (45 points)

You are given a digital system of 500 million transistors operated at 1.2V in 100nm process technology with gate capacitance of 1fF/micron and diffusion capacitance of 1fF/micron. The transistors are divided as follows

- 20 million are logic with average size of 12λ. Logic activity is 0.1.
- 480 million are memory with average size of 4λ. Memory activity is 0.05.

The process has two Vt voltages and two oxide thicknesses.
Sub-threshold leakage current for OFF device is:

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- 20nA/micron for low Vt
- 0.02nA/micron for high Vt

Gate leakage is:

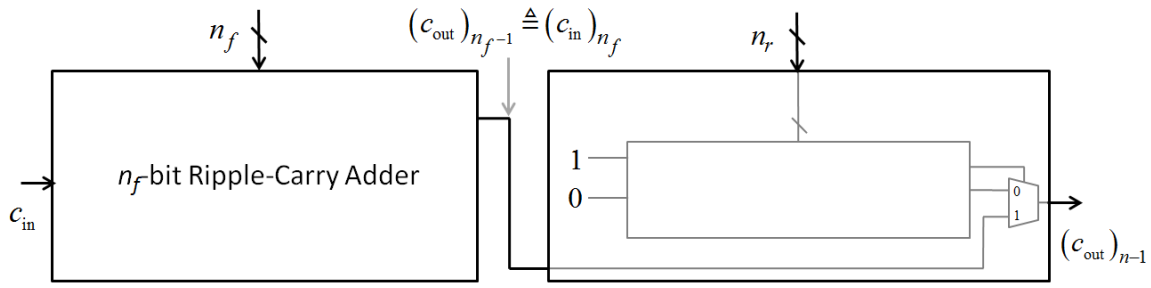
- 3nA/micron for thin gate oxide
- 0.002nA/micron for thick gate oxide

Memory uses low-leakage everywhere; logic uses low-leakage for 80% of its devices.

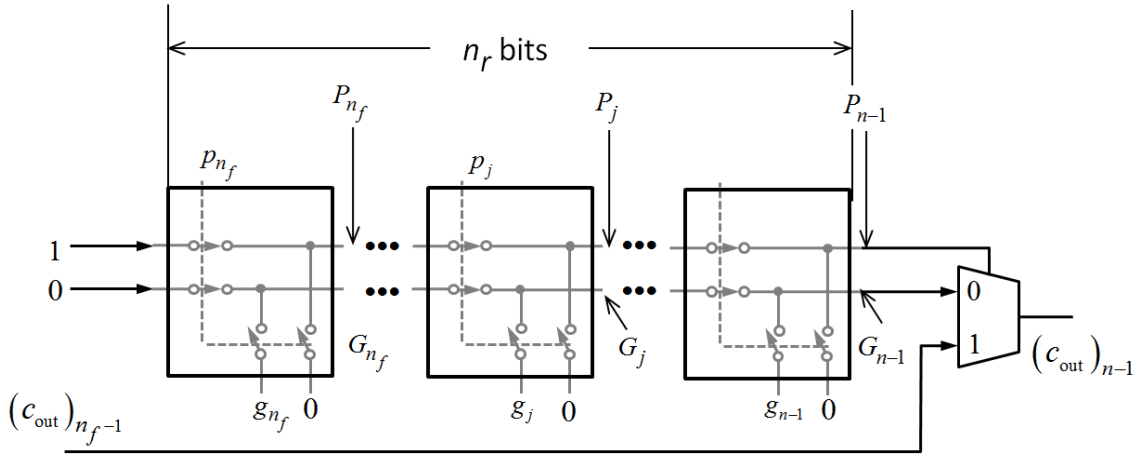
1. Neglecting wire capacitance, estimate the dynamic power consumption per MHz?
2. Estimate the static power. Explain step by step all your calculations and assumptions (if any).
3. What would be the static power if there were no low-leakage devices?
4. We wish to put two cores (chips) on a silicon die. It is assumed that switching power is 50% devices and 50% interconnects. What will be the maximal clock speed if we can afford 40W peak power dissipation?

Problem No 2 (75 points)

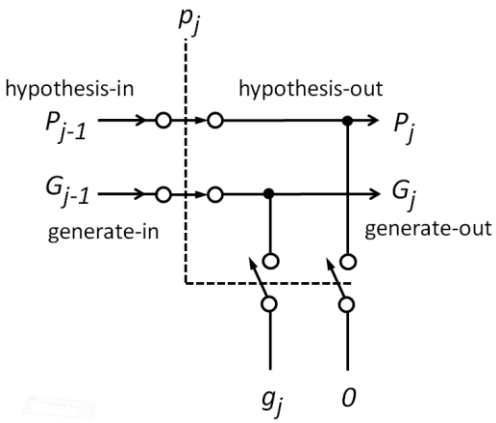
In order to speed-up addition, an n-bit adder comprising a mix of n_f-bit ripple-carry adder and n_r-bit carry-chain adder, $n = n_f + n_r$, is proposed as shown below. It is assumed that the signals $p_i = a_i \oplus b_i$ and $g_i = a_i b_i$, $n_f \le i \le n-1$ are available.



The internal design of the n_r -bit carry-chain is shown below.



The above chain consists of the following switches



1. Explain how speed-up is achieved.
2. Explain how the switch is working.
3. Implement the switch with appropriate transistors and explain your choice.
4. Write the expressions of the signals P_j and G_j . Explain the role of the MUX and elaborate how $(c_{out})_{n-1}$ is correctly computed.

5. What are the critical paths? How they depend on n_f and n_r?
6. Assume that the internal delay of a full-adder used in the ripple-carry is α, the on resistance of a switch is r and the capacitive load at switch nodes is c. Write the expression for which the worst-case delay is minimized.
7. What are the expressions of n_f and n_r at the minimum?
8. How the delay of the carry-chain depends on n and n_r?