BAR-ILAN UNIVERSITY (RA)

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אוניברסיטת בר-אילן (ע"ר)

בית הספר להנדסה

רמת-גן 52900

9 פברואר 2012 **פרופ' שמואל וימר**

מבוא לתכנון מעגלי VLSI

תשע"ב סמס' א' מועד א'

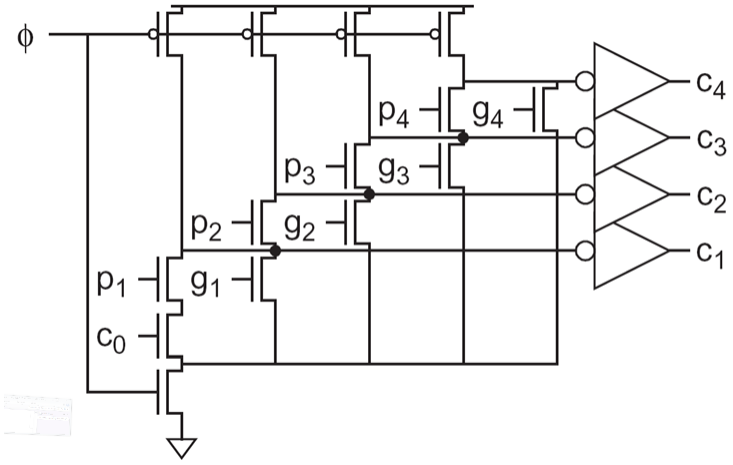
- יש לענות על כל השאלות. משקל השאלות השונות נתון בגוף השאלות.
- **יש לנמק את כל תשובותיכם**. אין צורך לפתח מחדש תוצאות שהוכחו בכיתה, אלא אם כן נאמר מפורשות לעשות כן.
- משך המבחן שלוש שעות (ע"פ תקנות האוניברסיטה לא תנתן הארכה).
- יש לשרטט מערכות ודיאגראמות באופן ברור !
- סך כל הנקודות הוא 120, הציון המירבי בכל מקרה לא יעלה על 100.
- השמוש בכל חומר כתוב (ספרים, רשימות) מותר .השמוש במחשב או בכל אמצעי אלקטרוני אחר אסור בהחלט.

בהצלחה

Problem No 1 (50 points)

The following CMOS circuit is performing some logic functions. Its inputs are c_0, p_i and g_i, and outputs are c_i, 1<=i<=4. Φ is a symmetric clock signal.

Assume size 4 of all n-type transistors involved in logic computations (evaluation).

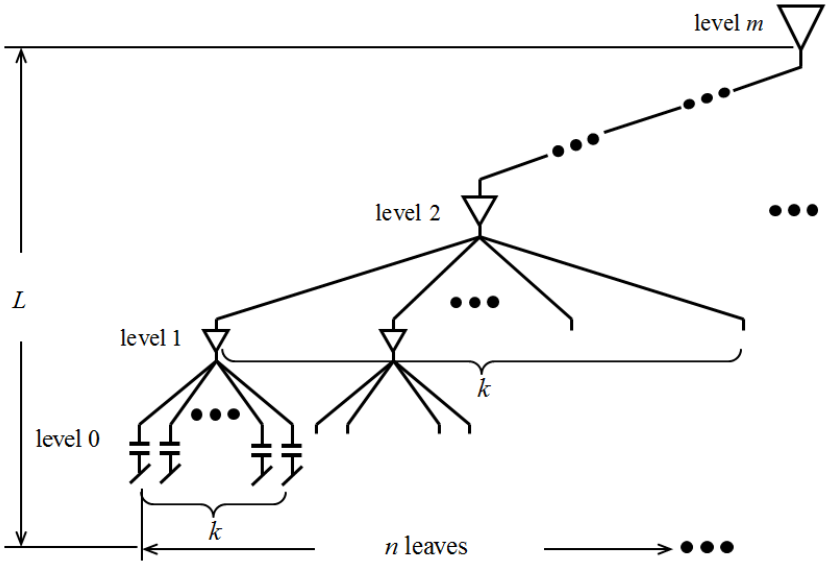


1. Explain how the circuit operates when Φ=0 and Φ=1.
2. Write the equations of the outputs as functions of the inputs.
3. What is the purpose of this circuit?
4. You are required to design the circuit in the most efficient way to yield best timing, with minimum power and area. What should be the size of the p-type transistors connected to Φ? Explain in details.
5. What is the critical path in this circuit? What transistors are involved? Explain in details.
6. Assume that the critical output is driving a similar circuit. What should be the size of the p-type and n-type transistors of that inverter?
7. Find the input-to-output delay of the critical path in terms of unit transistor resistance R and capacitance C. Use Elmore lumped delay model. Elaborate your calculations.
8. What is the maximum clock cycle this circuit can operate? (Express in terms of R and C.)

Problem No 2 (40 points)

A signal tree driving $n=k^m$ capacitive loads c_0 is shown below. The distance from the driver to every receiver is L, and we assume full symmetry and identity of every path from driver to receiver.

- The wire connecting the last driver to the load has resistance ***R*** and capacitance ***C***. Wires of successive levels has same length growing factor ***s*** and width sizing factor ***β***.
- The last driver has resistance ***r*** and input and output capacitances ***c***. Drivers are sized from level to level by factor ***α***. The internal delay of all drivers at all levels is ***d***.
- The capacitive load of a leaf is c_0, namely, the last driver drives kc_0 load.



1. What is (are) the critical path (s)?
2. Write the appropriate delay expression. Use Elmore lumped and distributed delay models appropriately.
3. Assuming ***β*** =1, find the optimal sizing factor ***α*** of a driver such that the delay from driver to leaf load is minimized.
4. Assuming ***α*** =1, find the optimal sizing factor ***β*** of a wire such that the delay from driver to leaf load is minimized.
5. What are ***α*** and ***β*** that minimize the delay from driver to leaf load?
6. Assume that power is the only interest. How would you then determine ***α*** and ***β***?
7. Assume that area is the only interest, how would you determine ***α*** and ***β*** then?

Problem No 3 (30 points)

We wish to perform unsigned multiplication $P=11101101_2 \times 01100101_2$ in radix-4 Booth-encoded multiplier.

1. Write the partial products. Elaborate your computations step by step in details.

2. Fill in the corresponding dot diagram with the appropriate values.