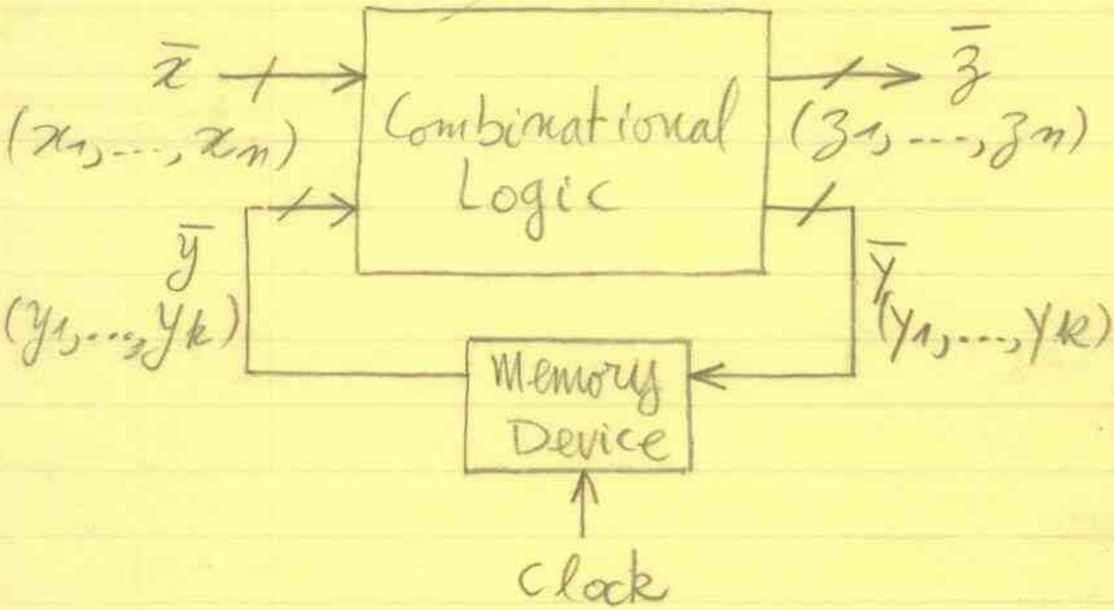
8

Synchronous Sequential Circuits



Clock pulses mask all delay effects

$$Y_i(t+1) = G_i(\bar{x}(t), \bar{y}(t)) \quad i=1,2,\ldots,k$$

$$z_i(t) = F_i(\bar{x}(t), \bar{y}(t)) \quad i=1,2,\ldots,m \quad \text{Mealy}$$

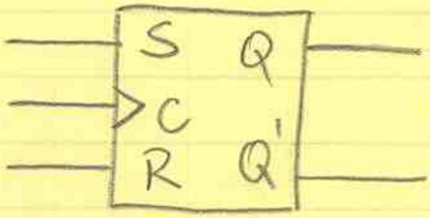
$$z_i(t) = F_i(\bar{y}(t)), \quad i=1,2,\ldots,m \quad \text{Moore}$$

t and $t+1$ are two consecutive clock pulses.

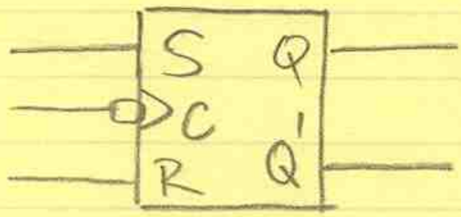
While Latches are transparent FlipFlops are bistable devices gated by clocks.

SR FlipFlop - edge triggered

Works similar to gated SR Latch, where Enable is clock (Positive edge triggered) or clock' (negative edge triggered)



positive edge triggered



negative edge triggered

$$Q(t+1) = R'Q(t) + S \qquad SR = 0$$

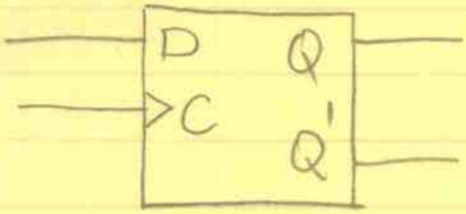
S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	לא מוגדר

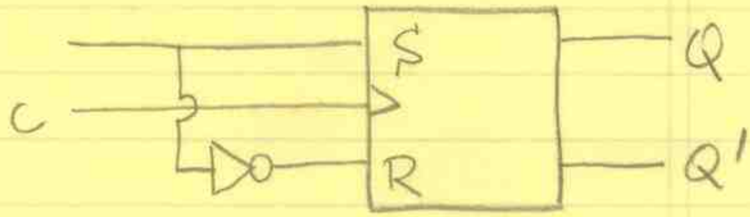
reduced characteristic table

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation table

D Flip Flop - edge triggered





Implementation

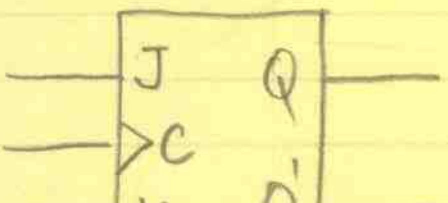
D	Q(t+1)
0	0
1	1

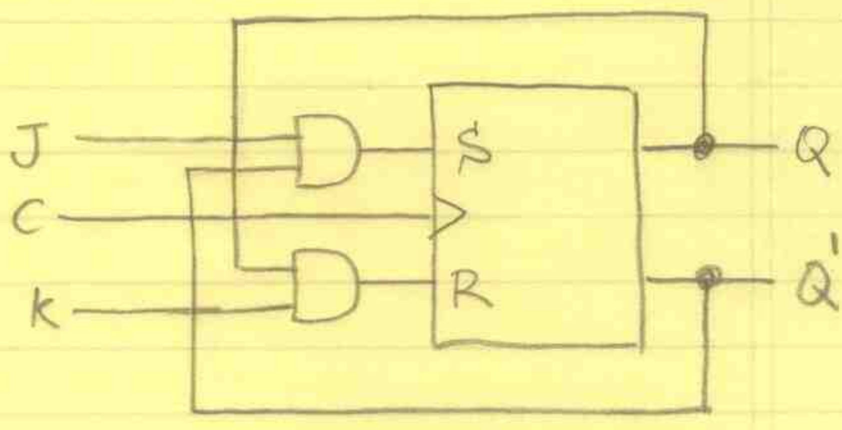
reduced characteristic table

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table

Jk Flip Flop - edge triggered





Implementation

Unlike pure SR,

Jk output is determined for J=1 k=1

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

Reduced characteristic table

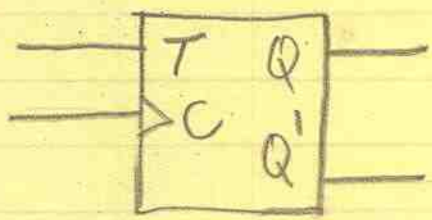
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

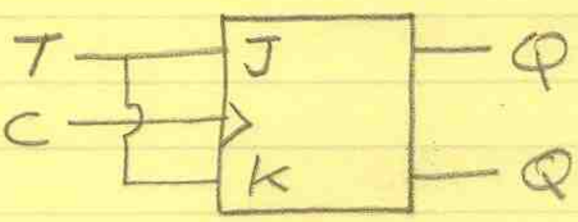
Excitation table

$$Q(t+1) = K'Q + JQ'$$

T Flip Flop - edge triggered

Obtained from JK FF by connectig J and K





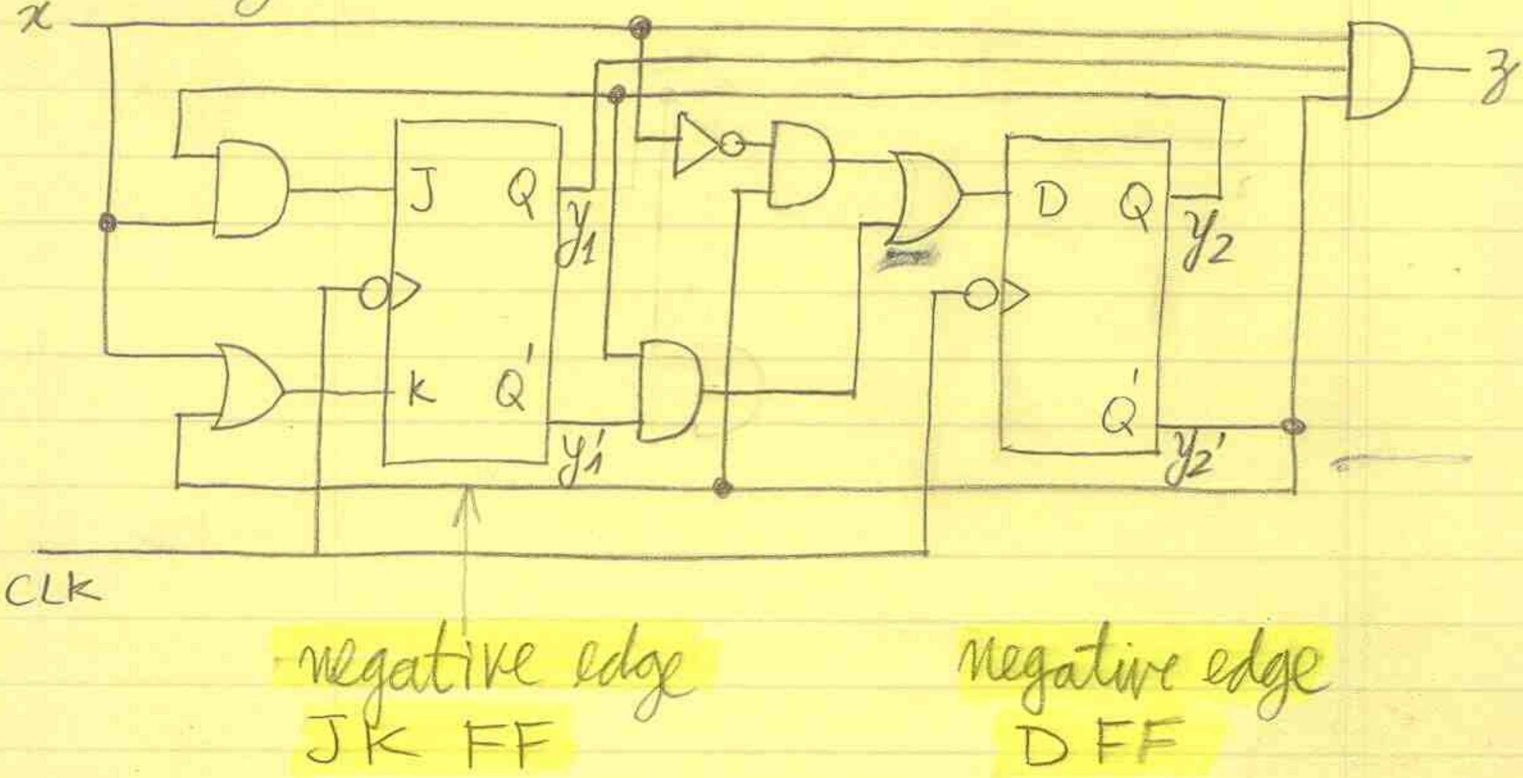
T	Q(t+1)
0	Q(t)
1	Q'(t)

characteristic table

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

exitation table

Analysis Example



Above circuit has $y_1 y_2$ states variables, hence there are 4 states 00 01 11 and 10

① Exitation equations

$J = x y_2$ $\quad K = x + y_2'$ $\quad D = x' y_2' + y_1' y_2$

PS $y_1 y_2$	$x=0$ J	K	D	$x=1$ J	K	D
00	0	1	1	0	1	0
01	0	0	1	1	1	1
10	0	1	1	0	1	0
11	0	0	0	1	1	0

Exitation table

② Output equations

$$z = x y_1 y_2'$$

PS	z	
$y_1 y_2$	$x=0$	$x=1$
00	0	0
01	0	0
10	0	1
11	0	0

③ Next state equations

They are derived by subsituting the excitation equations of each FF into its characteristic equation

JK FF: $Q(t+1) = K'Q + JQ'$

$$\Downarrow$$

$$Y_1(t+1) = (x+y_2')'y_1 + (xy_2)y_1' = x'y_1y_2 + xy_1'y_2$$

D FF: $Q(t+1) = D$

$$\Downarrow$$

$$Y_2(t+1) = x'y_2' + y_1'y_2$$

(4) State table

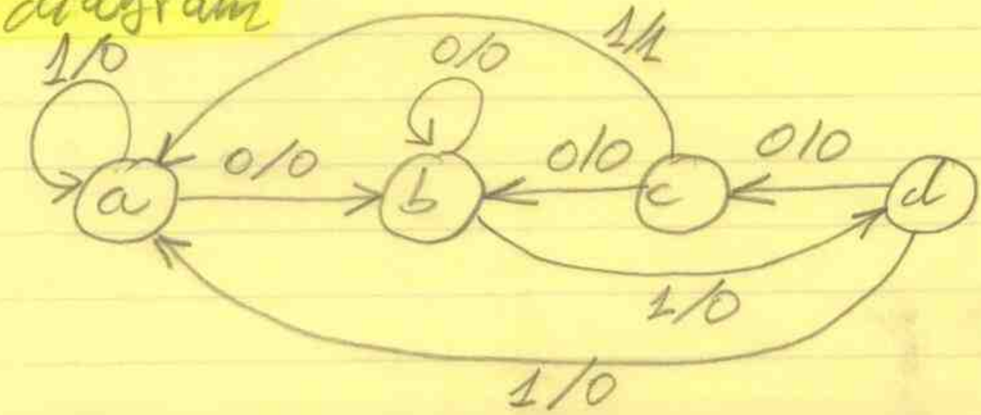
set symbols to states

a=00 b=01 c=10 d=11

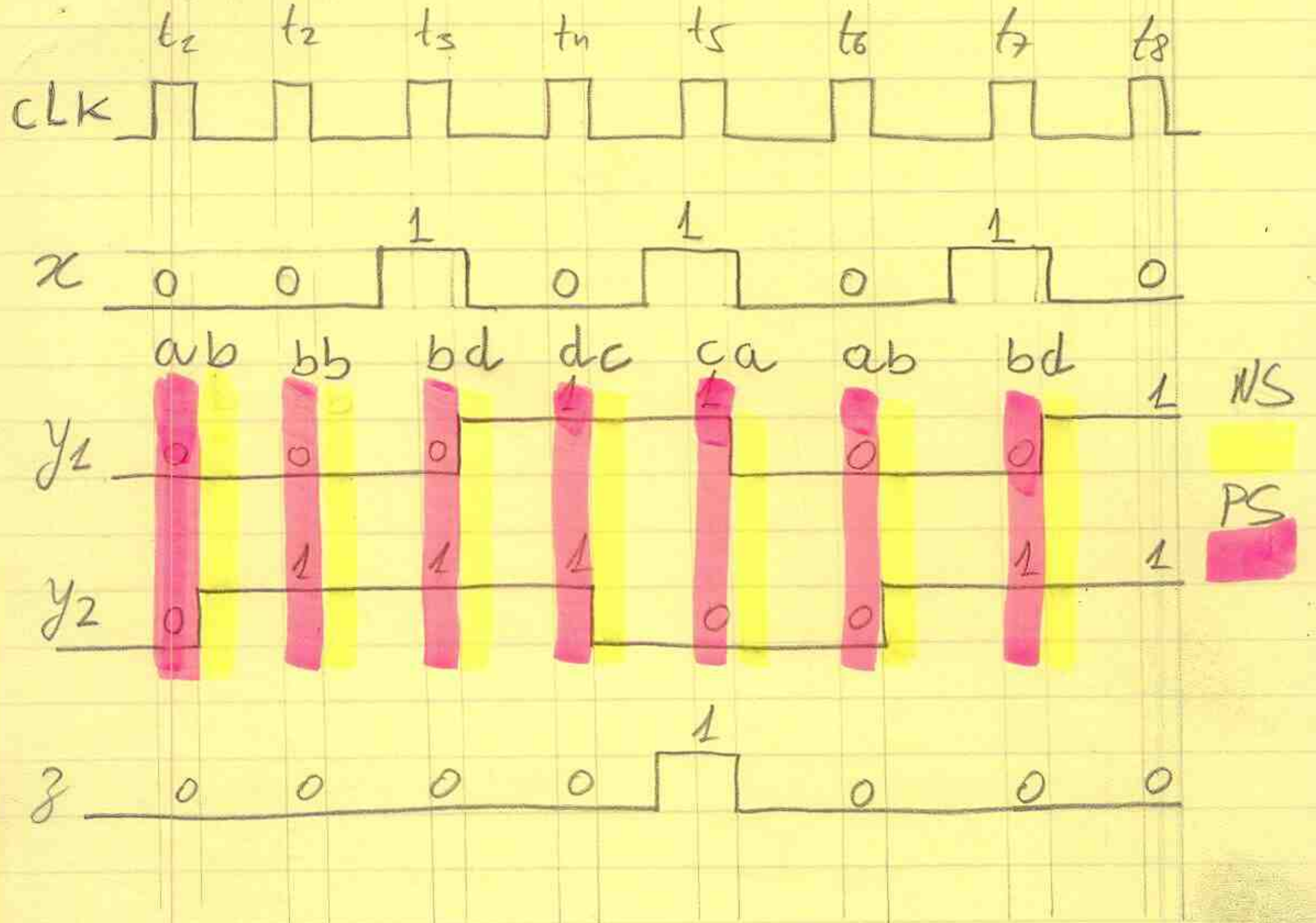
PS y_1y_2	$NS(Y_1Y_2)$ / Output (z) $x=0$	$x=1$
00	01/0	00/0
01	01/0	11/0
10	01/0	00/1
11	10/0	00/0

PS y_1y_2	NS/Output (Y_1Y_2/z) $x=0$	$x=1$
a	b/0	a/0
b	b/0	d/0
c	b/0	a/1
d	c/0	a/0

(5) State diagram



⑥ Timing diagram



Comments:

- Timing diagram is ideal, no propagation delay
- Input counts for setup time and hold time
- Transitions on negative edge
- input vs output 0 0 1 0 1 0 1 0
  0 0 0 0 1 0 0 0

- This state machine discovers 0101 sequences.
- Present state is read before transition, while
- next state occurs after transition edge

Design example - Filter

Design spec:

Input is a sequence of 0's and 1's.

The output starts on the same value as input and changes its value only if a sequence of 3 consecutive pulses of opposite value occurs. Namely, the circuit filters sequences of length shorter than 3

input x: 0 0 1 0 1 0 1 1 1 0 0 0 1 1 1 0 1

output z: 0 0 0 0 0 0 0 0 1 1 1 0 0 0 1 1 1

x: 1 1 0 0 0 0 1 0 1 1 1 0 1 0 0 0 0

z: 1 1 1 1 0 0 0 0 0 0 0 1 1 1 1 0 0

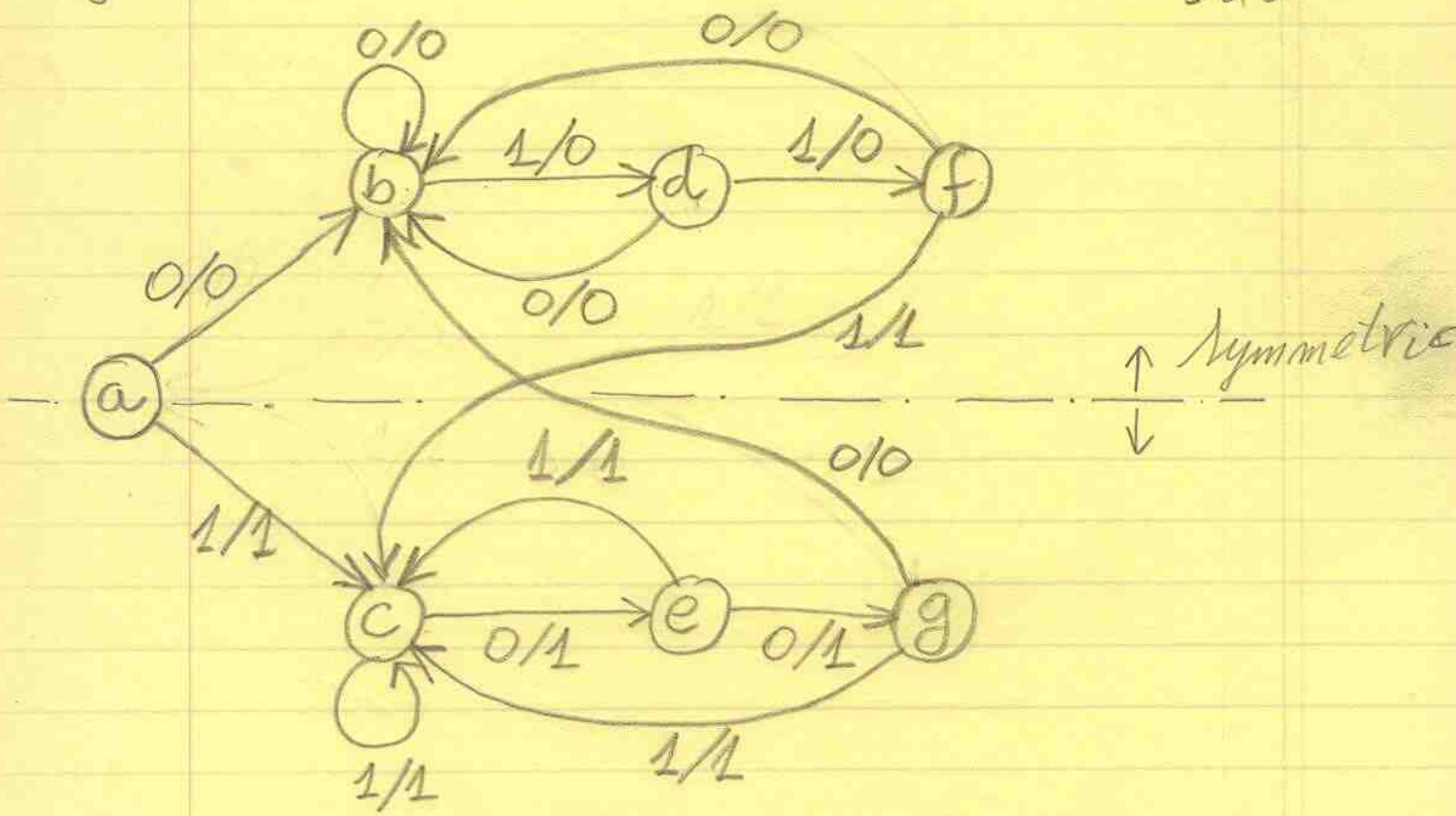
Step ①: State diagram and table

ⓐ - Initial state, on 0 goto ⓑ, on 1 goto ⓒ

ⓑ - Reporting steady 0 sequence - output 0
ⓒ - " " 1 " - " 1

ⓓ - Indicate 1st 1 - output 0
ⓔ - " " 0 - " 1

ⓕ - Indicate 2nd 1 - output 0 $\xrightarrow{\text{3rd 1}}$ ⓒ
ⓖ - " " 0 - " 1 $\xrightarrow[\text{3rd 0}]{}$ ⓑ



Symmetry! - good sanity check!

PS	NS / output (z) $x=0$	$x=1$
a	b/0	c/1
b	b/0	d/0
c	e/1	c/1
d	b/0	f/0
e	g/1	c/1
f	b/0	c/1
g	b/0	c/1

step ② - State reduction

a, f and g are equivalent {a, f, g}, {b}, {c}, {d}, {e}

PS	NS/ Output z $x=0$	$x=1$
a	b/0	c/1
b	b/0	d/0
c	e/1	c/1
d	b/0	a/0
e	a/1	c/1

Step ③ - State assigment

Assignment requires 3 state variables and is arbitrary (Synchronous) unlike Asynchronous where race-free assigment is in order

PS $y_1y_2y_3$	NS($Y_1Y_2Y_3$) / Output z) $x=0$	$x=1$
000	001/0	010/1
001	001/0	011/0
010	100/1	010/1
011	001/0	000/0
100	000/1	010/1

Step ④ - Next state and output equations

y_1y_2 \ y_3x	00	01	11	10
00	0	1	0	0
01	1	1	0	0
11	X	X	X	X
10	1	1	X	X

$$z = y_1 + y_3'x + y_2y_3'$$

y_1y_2 \ y_3x	00	01	11	10
00	1	0	1	1
01	0	0	0	1
11	X	X	X	X
10	0	0	X	X

$$Y_3(t+1) = y_1'y_2'x' + y_3x' + y_2'y_3$$

$Y_1(t+1)$ and $Y_2(t+1)$ are derived similarily

$$\left.\begin{aligned} Y_1(t+1) &= y_2y_3'x' \\ Y_2(t+1) &= y_2'x + y_3'x \end{aligned}\right\} \text{Homework}$$

Step 5 FlipFlop exitation equations

No general algorithm to decide on type of FF.

We use JK FF

$$Q(t+1) = K'Q + JQ'$$

$$Y_1(t+1) = y_2y_3'x' = (y_2y_3'x')y_1 + (y_2y_3'x')y_1'$$

$$\Rightarrow K_1 = y_2' + y_3 + x \quad , \quad J_1 = y_2y_3'x'$$

$$Y_2(t+1) = y_2'x + y_3'x = y_2'x + y_2y_3'x + \cancel{y_2'y_3'x} =$$

absorption

$$= (y_3'x)y_2 + (x)y_2'$$

$$\Rightarrow K_2 = (y_3'x)' = y_3 + x', \quad J_2 = x$$

$$Y_3(t+1) = y_1'y_2'x' + y_3x' + y_2'y_3 =$$

$$y_3(\cancel{y_1'y_2'x'} + x' + y_2') + y_3'(y_1'y_2'x') =$$

absorption

$$= (x' + y_2')y_3 + (y_1'y_2'x')y_3'$$

$$\Rightarrow K_3 = (x' + y_2')' = x \cdot y_2, \quad J_3 = y_1'y_2'x'$$

alternatively, exitation table conditions can be embeded directly into state transition table and then use K-map for each K_i and J_i

$Q(t)\ (y_i)$	$Q(t+1)\ (Y_i)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

PS	NS ($Y_1Y_2Y_3$)		$x=0$					
$y_1y_2y_3$	$x=0$	$x=1$	J_1	K_1	J_2	K_2	J_3	K_3
000	001	010	0	X	0	X	1	X
001	001	011	0	X	0	X	X	0
010	100	010	1	X	X	1	0	X
011	001	000	0	X	X	1	X	0
100	000	010	X	1	0	X	0	X

$x=1$

J_1	K_1	J_2	K_2	J_3	K_3
0	X	1	X	0	X
0	X	1	X	X	0
0	X	X	0	0	X
0	X	X	1	X	1
X	1	1	X	0	X

We can build K-maps $J_i(y_1, y_2, y_3, x)$ and $K_i(y_1, y_2, y_3, x)$ $i=1,2,3$ and derive excitation equation for each FF - Homework. This may yield simpler excitation equations

J_1 map

$y_1y_2 \backslash y_3x$	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	X	X	X	X
10	X	X	X	X

$J_1 = y_2 y_3' x'$

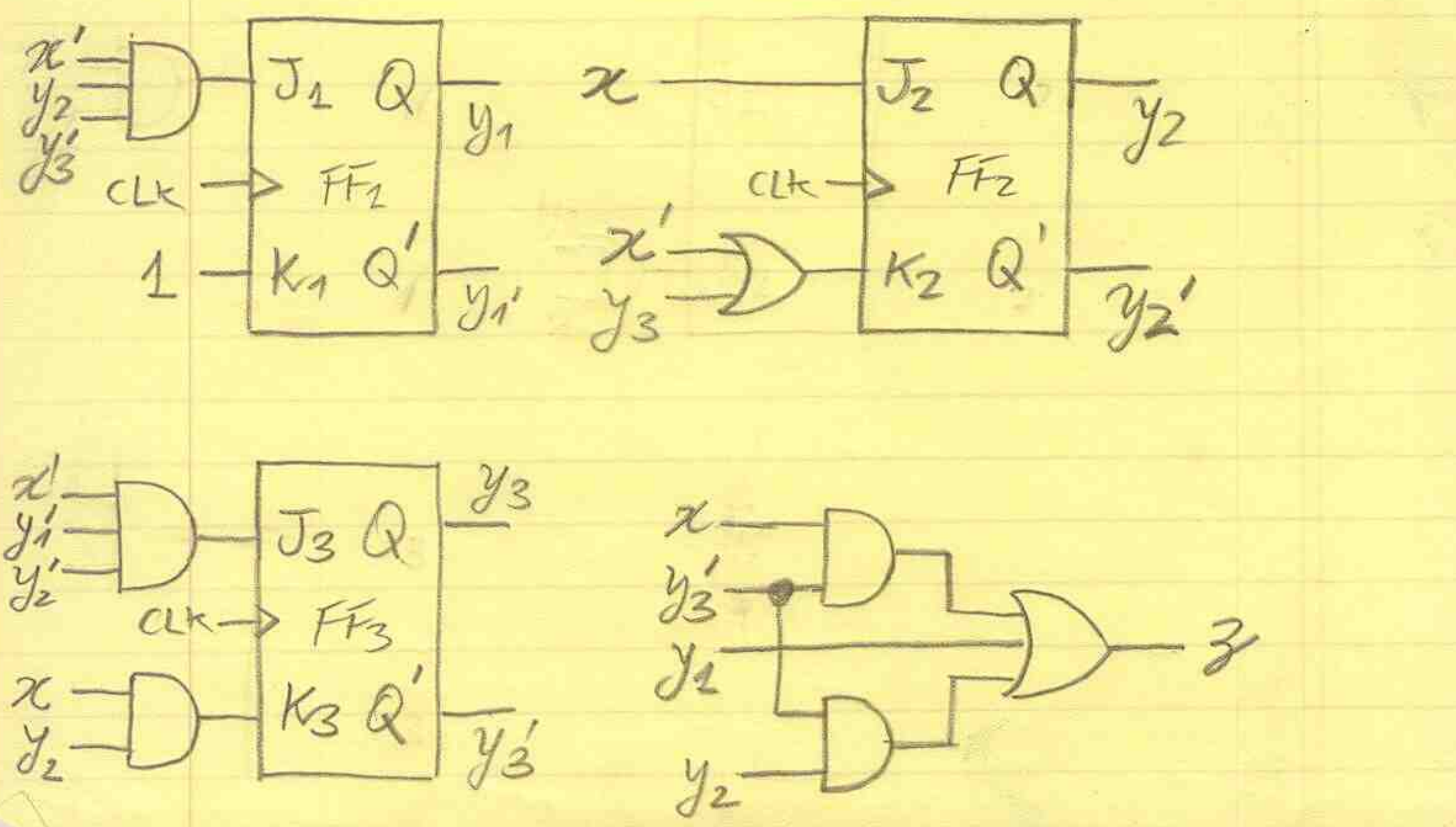
K_1 map

$y_1y_2 \backslash y_3x$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$K_1 = 1$

(Simpler than $y_2' + y_3 + x$)

Step ⑥ - Circuit Logic diagram



Important:

1- Circuit works properly if it preset to its initial state 000. This requires asynchronous inputs to FF (not studied)

2- If upon initialization in any of the invalid states (unused codes) the circuit goes to valid state (used code) within few pulses, this is called self-starting, which is okay but must be validated.

3- Otherwise, all unused states must be assigned with valid next state (e.g. a-000) on the expense of giving up the don't care (more complex exitation equations)

Homework: Verify self-Starting from exitation equation