Post Optimization of a Clock Tree for Power Supply Noise Reduction

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***Abstract*—The voltage drop incurred in the power supply in today's VLSI chips to is a major concern known as power-supply noise. In sub one-volt supply voltage, noise of very few hundreds millivolts causes circuit malfunction. The reason for power supply noise is the fast and simultaneous transistor switching. While the logic signal switching is spread across the entire clock cycle, the switching of the clock tree and the sequential circuits are occurring simultaneously, causing high local current peaks. The clock related transistor switching is the primary contributor to power supply noise. This paper proposes to spread the switching of clock tree drivers in an attempt to reduce the peak-current, while maintaining the clock signal quality and low skew at the far end tree's leaves where the sequential circuits are connected. A methodology of cell switching characterization was developed for fast computation of peak-current and other signals parameters. This computation is embedded in a branch and bound tree traversal. We propose a novel optimization algorithm based on clock tree delay-invariant branch transformation, replacing low-threshold by high-threshold and smaller size drivers. The algorithm was implemented in 40 nanometers design. We achieved a reduction of 50% of clock-tree peak-current..**

I. Introduction

The voltage drop incurred in the power supply in today's VLSI chips to is a major concern known as power-supply noise [1]. With the increase of design complexity, moving from ASIC to System on a Chip (SoC), and due to the sub one-volt supply voltage, noise of very few hundreds millivolts causes circuit malfunction. The clock related voltage switching is the primary contributor to power supply noise [2]. A well-structured clock-tee should deliver high quality clock signal to the underlying sequential circuits connected at tree's leaves. The clock skew must stay within certain limits to ensure proper and robust sequencing of the logic. To ensure fast switching of the logic, the slew of the signal at tree's leaves must also be small enough. The attempt to reduce the peak-current drawn from the power supply by clock-tree treatment is therefore a delicate task which must be handled carefully to ensure clock signal integrity.

Ordinary logic and sequential circuits are designed to work in nominal power supply voltage. Unfortunately maintaining constant voltage during operation is simply impossible. The power network is an RLC circuit and high current peaks will cause various voltage drops at various points of the network. (see Fig 1).

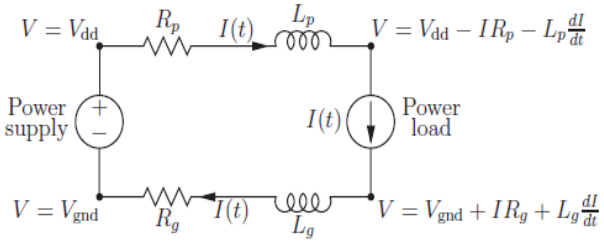

Figure 1. IR drop components based on RLC of Power Distribution Network (PDN) and transistors who are Power load of a SoC

Once process variability and ambient conditions come into consideration this phenomenon is significantly increasing [2]. It all comes to the simple Ohm low of multiplying peak-current value by the power network impedance. The noise can therefore be reduced by either lowering the impedance, or avoiding high peak-current. Constructing proper power supply network having low-resistance and inductance, and high capacitance has been treated in many research papers [3] and is beyond the scope of this paper.

Peak-current reduction achieves the following goals:

- It is reducing the IR drop on die, where the resistance is the major impedance factor.
- It is reducing the $L(dI/dt)$ term occurring at the package level, where inductance is a predominant impedance factor.
- Clock jitter is being reduced since it is directly affected by IR drop.
- It causes better utilization of the de-coupling capacitors since it is reducing the distance of the effective capacitors used to mitigate the voltage drop. This distance is increasing with dI/dt reduction.

The rest of this paper is organized as follows. Section 2 describes the structure of a clock-tree, describing the buildup of the power-supply noise and highlighting the theme of this work. Section 3 presents a clock-driver characterization method that is a central component in the computational

efficiency of the peak-current reduction algorithm, elaborated in Section 4.

II. Clock-tree and power-supply noise

Fig.2 illustrates the clock H-tree used by PowerPC processors family [4].

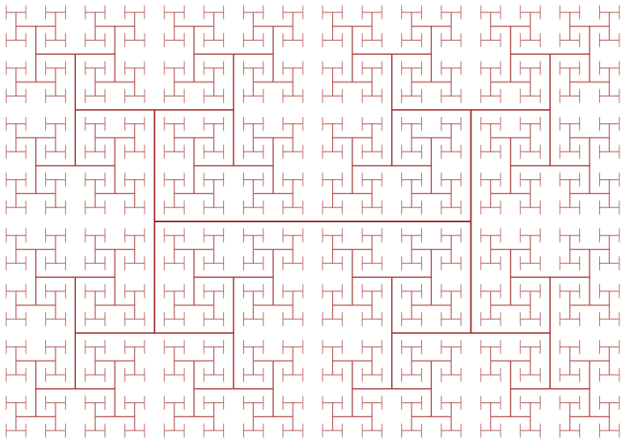

Figure 2. Clock network H-tree diagram

Its inherent symmetry made it favorite for distributing robust clock signals. By its very structure, each sink (tree's leaf) has similar path to root, comprising similar drivers and interconnecting segments. This ensures (up to on-die variations) same nominal source-to-sink latency, and hence clock-skew is remains very small (nominally). The elegancy of the H-tree structure is also a source of considerable power-noise. Due to its symmetry, all the drivers at a given level of the tree will switch simultaneously. This result in a progressive sequence of current peaks, cumulating to a current pulse whose amplitude is increasing as we progress from source (tree's root) down to sinks (tree's leaves), as depicted in Fig. 3. Flattening of the cumulative current shape will reduce both chip-level and package-level noise. The former due to IR voltage drop reduction, while the latter which is governed by $L(dI/dt)$ is also reduced due to the smoothing of the current pulse profile. It is important to note that the amount of current over time (charge) is unchanged, namely, the consumed power and energy are unchanged.

To ensure robust signal with low slew, the clock-tree is traditionally using low or nominal threshold voltage transistors, called in VLSI jargon LVT and NVT, respectively. Though suffering of high leakage, their short transition time ensures low slew of the clock signal at the sinks. Moreover, the uniformity of clock-tree structure, where each level of the tree comprises identical drivers ensures that signal uniformly propagates to sink. This causes that the skew at each tree's level being small enough such that small skew is guaranteed at tree's sinks, where FFs are connected. The robustness of the clock signal at tree's internal nodes does not stand for itself; it is serving the integrity requirements at sinks. So an important question is whether this uniformity can be given up, provided that the integrity at leaves is achieved.

Here lies the idea of our proposal which breaks this paradigm.

- Replace as many as possible of the LVT and NVT drivers by LVT ones.
- Blend various types in the same level of the tree to introduce some "randomness" into tree.
- Use mix of driver sizes at the same level of the tree, providing another degree of "randomness".
- Maintain acceptable clock signal slew and skew at sinks.

III. Characterization of clock drivers

The combinatorial algorithm minimizing the peak current is traversing the clock-tree T in a branch-and-bound manner, where each visited node is evaluating its peak current, signal delay and its slew. Those values are used to decide whether backtracking should take place. Evaluating those parameters by a simulation at each node is unacceptable due to the impractical total computation time. Rather, we could beforehand characterize each clock driver and then use composition of characteristics which is far computational efficient than simulation. It will be sown that only little accuracy is sacrificed compared to simulation.

The build of the clock-drive characterization library takes place offline. We first define the repertoire of library drivers. Each driver is then characterized by running extensive spice transient simulations whose results are tabulated for further use in the branch-and-bound algorithm. We demonstrate the algorithm on 40 nanometers process technology design. For the sake of demonstration the diver library is characterized in a PVT corner where $P = \text{Typical}$ (process is typical), $V_{\text{dd}} = 1.1V$ and $T = 25^{\circ}\text{C}$. Similar characterization can take place in other corners as well.

Characterization is using two inputs:

1. A vector of input slew values called $Slope_{\text{in}}$, given in picoseconds, $Slope_{\text{in}}$: (8, 28, 48, 68, 88, 108,128, 148, 168, 188, 208)
2. A vector of capacitive load values called C_{L}, given in femtofarads, C_{L} : (5, 35, 65, 95, 125, 155, 185).

Each pair of slew-load $(s,c) \in Slope_{\text{in}} \times C_{\text{L}}$ is simulated by SPICE to obtain the following set of tabular functions characterizing driver's behavior under input variables.

1. $Slope_{\text{out}}(s,c)$ -measured from 10% to 90% of V_{dd}.
2. $T_{\text{pd}}(s,c)$ -50% to 50% propagation delay.

Three peak current related parameters incurring at switching are specified below:

3. $I_{\text{peak}}(s,c)$-current peak in milliamps incurring during the cell switching.
4. $T_{\text{peak}}(s,c)$-the time elapsed from switching start until I_{peak} occurred.
5. $T_{10\%\ \text{peak}}(s,c)$-the time elapsed from switching start until 10% of I_{peak} occurred.

Additional parameters are measured.

6. $Energy_{\text{switch}}(s,c)$-the energy in picojoule consumed by driver switching.
7. I_{leakage}-driver's leakage current.

IV. The Replacement of LVT by HVT Drivers

Clock-tree peak current reduction is achieved by deteriorating tree uniformity in an attempt to spread the switching time at a level, thus avoiding aligned switching. The optimization algorithm is replacing LVT by HVT drivers. This has two advantages. Firstly, due to its longer T_{pd}, the coherency of the switching time at a level will be disrupted. Secondly, a by-product is the reduction of leakage current. Though it does not affect the power noise, it has the benefit of total power and energy reduction. A hazardous situation is immediately arising. Isn't that such replacements result in a diverse of propagation delays along root-to-leaf paths, which eventually may take clock skew out of prescribed value? As simple driver transformation which avoids this problem is subsequently described.

Consider a clock-tree initially designed as shown in Fig. 3, comprising LVT drivers, which is the common design practice. Fig. 4 shows the result of a SPICE simulation of a step input response obtained for the illustrated drivers.

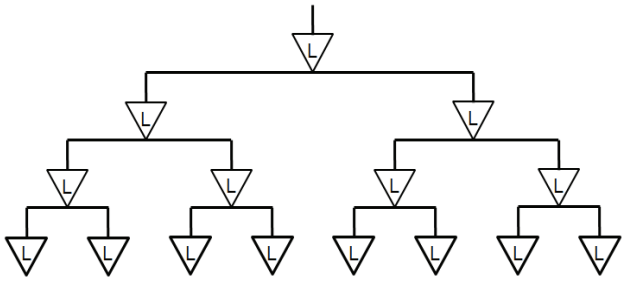

Figure 3.Clock-tree comprising LVT drivers.

The green curve is the response of an HVT driver and the red curve is the response of two cascaded LVT drivers of half size of the original LVT. We denote the latter by LVT/2. Expectedly, rise time of the latter is faster. However the 50% to 50% delay difference between the two configurations is 3.6 picoseconds, which is less than 0.5% of 1GHz clock frequency. Same behavior was observed in simulations for the entire driver cell library in 40 manometers technology.

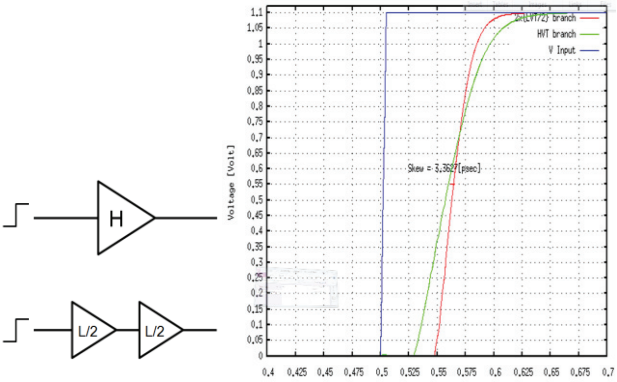

Figure 4. Step response for two driver configurations

The simulation below shows the impact on peak current resulted by HVT and LVT/2 driver replacements. Fig.5 is the current waveform occurred by ordinary (default) 2 LVT drivers. The green waveform in Fig. 6(a) is obtained for HVT while the red one results from cascaded LVT/2. Their superposition is shown in Fig 6(b). Comparing Fig. 6(b) with Fig 5, the current peak was reduced by 43%.

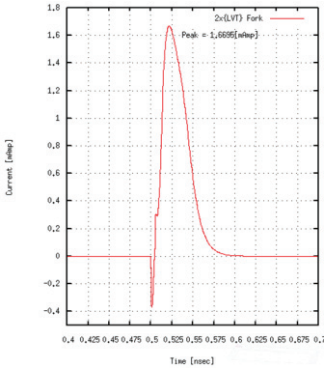

Figure 5.The peak current behavior of two LVT buffers

We shall subsequently take advantage of this behavior by replacing the full-size LVT drivers initially existing in the tree, by either of the driver configurations in Fig. 5. As shown later, the peak current drown by the root of the tree will be cut by half, while the skew at leaves will remain in the prescribed specification.

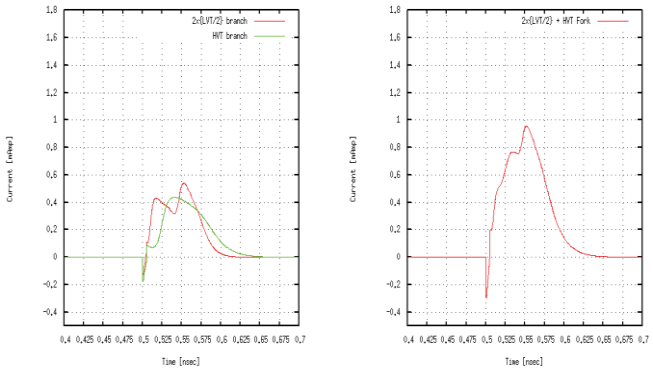

Figure 6 .The impact of driver transformation on peak current.

Left -6(a), right-6(b).

The main steps of our greedy peak-current minimization algorithm are the following:

1. Initialization: replace all LVT cells by two cascaded LVT/2 ones.
2. Traverse the tree in pre-order. At the currently visited node do the following:
   a. Examine both driver configurations.
   b. For each configuration calculate the cumulative delay from root.
   c. Update the current waveform by superposition.
   d. Calculate the slew at the output of the driver.
3. Once a leaf is encountered, select the optimal solution in hand, thus fixing the driver configuration along the root-to-leaf path.

It follows from the logarithmic depth of the tree that for a tree of n leaves there are $O(n)$ ($O(n^2)$) optional solutions, among which the best one is selected. Moreover, some of those are discarded during the incremental construction along the root-to-leaf paths by slew criteria. This is necessary due to the greedy nature of the minimization algorithm which is blind to later traversed paths and must therefore ensure that slew at internal nodes of root-to-leaf paths will not escape. A precise definition of the optimization cost and constraints is described later. A key feature of this algorithm its computational efficiency. Not only that the solution space is linear (quadratic) in the size of the problem, but the computations at each node are done accurately and efficiently by static calculations based on driver characteristics obtained beforehand.

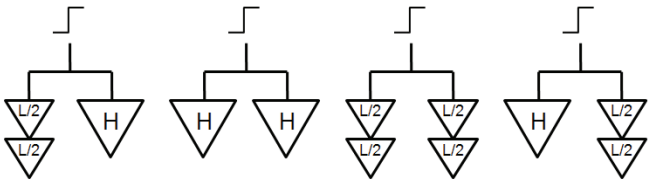

Figure 7 .Possible driver replacements at a node.

A delicate point of the pre-order traversal needs further discussion. The traversal is augmenting paths by considering each of the four possible configurations shown in Fig. 7. Clearly, augmentation must consider both left and right branches simultaneously, as otherwise the real load at the parent is unknown and accurate delay, slew and current profile computations will not be possible. Consequently, whenever the pre-order traversal is progressing to a left sub-tree, the first branch of the right tree is also decides. Once a leaf is reached and a decision on driver implementation along the path takes place, the left branches that are subject to a decision imply commitment of the sibling branches. Considering a root-to-leaf pats as shown in Fig. 8, let ρ be its root, μ be a leaf, and ω is the lowest level node along the path where a right turn took place. The nodes along the paths can be characterized as follows.

1. From ρ up to ω, excluding. The implementation of being either HVT or cascaded LVT/2 has already been determined and fixed for those nodes.
2. From ω up to a leaf μ. The driver implementation of those nodes is not determined yet. Upon visit, any of the four driver configurations in Fig. 4 is examined and the relevant parameters are calculated for the left and tight son.

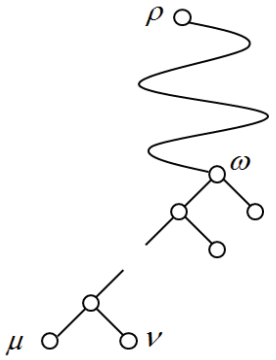

Figure 8 .A root-to-leaf path of the modified tree.

Since at each node from ω up to a leaf μ, excluding, four paths augmentation possibilities are considered and recorded for further decision of the optimal solution, the amount of possible paths implementation is $O\left(4^{\log_2 n}\right) = O\left(n^2\right)$.

V. DISCUSSION AND CONCLUSIONS

As it was noticed before clock tree is one of the major contributors of peak current in a SoC, that circumstance cannot be neglected and should be treated. Here we introduced one of the possible solutions. In that paper we didn't consider the impact of the process variation and differentiation of temperature among the SoC. All these effects will harm and affect negatively on jitter and skew of the optimized clock tree.

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