Adam Teman

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Emerging Nanoscaled Integrated
Circuits & Systems Labs (EnICS)
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Research Interests

VLSI Memory with a focus on energy efficiency, leakage reduction, stability, robustness, and yield improvement, and in-memory computing, including:

- SRAM design for low-voltage, low-power operation, data retention voltage analysis, static and dynamic noise margins and stability, dealing with process variations and radiation noise, and internal feedback mechanisms.
- Embedded DRAM design, as an alternative for SRAM in low-power embedded systems, such as biomedical sensors, and in high bandwidth systems.
- Novel in-memory computing architectures and techniques for Artificial Intelligence applications.
- Integration of memory with on-chip sensors, including peripheral sharing for power and area reduction.
- Development of alternative memories: FeRAM, PCM, MRAM, Memristors, CNT/Graphene based memory, etc.

Energy-Efficient Circuit Design with an emphasis on:

- Subthreshold and near-threshold digital design of circuits and systems
- Library development, characterization, and selection for optimal operation.
- Approximate, significance-driven computing
- Error-resilient circuits and systems
- Efficient physical implementation methodologies for low-power
- Alternative, low-power variation tolerant logic families and digital gates
- Asynchronous circuits and components
- Feedback in digital systems
- Low-power image sensors and sensor arrays

Engineering Education, including methods for improvement of engineering pedagogy in Israel, implementation of knowledge conservation systems in research centers, and efficient integration of e-learning into university courses.

Employment History

Oct 2015–present
Senior Lecturer (Tenure Track Faculty)
Bar-Ilan University (BIU), Ramat Gan, Israel
• Senior Faculty member at Bar-Ilan University since October 2015.
• Co-director Emerging NanoScaled Integrated Circuits and Systems (EnICS) Labs Impact Center, BIU
• Academic Co-director System-on-Chip (SoC) Lab, EnICS Labs, BIU

Jan 2014–Oct 2015
Post-Doctoral Researcher/Scientist
École Polytechnique Fédérale de Lausanne (EPFL), Switzerland.
• Post-doctoral position in the TCL group led by Prof. Andreas Burg.
• Recipient of Swiss Government Excellence Scholarship for 2014.
• Participating in the FP7 SCoRPiO consortium, developing Significance-Based Computing for Reliability and Power Optimization. Specifically developing fault-tolerant processing core for energy efficient, variability aware, low-power operation in 28nm FD-SOI process.
• Participating in the icySoC NanoTerra consortium, developing inexact sub-threshold systems for ultra-low power devices. Specifically developing inexact accelerators and low-voltage standard cell memories for integration in the PULP platform.

2008–2014
Lecturer/Teaching Assistant/Researcher.
Ben-Gurion University of the Negev (BGU), Be'er Sheva, Israel
• Lead researcher on low-power VLSI arrays and memory circuits in the Low Power Circuits and Systems Lab of the VLSI Systems Center.
• Development and advancement of processes and flows in the VLSI Systems Center.
• Advisor to six MSc Theses and 17 Senior Projects
• Lecturer of eight semester long undergraduate courses and one semester long graduate course, including course development.
• Teaching assistant of four semester long undergraduate courses.
• Lab assistant during three semesters.

2006–2007
Backend/Design Engineer.
Marvell Semiconductor Ltd., Yokne'am, Israel
• Part of the design team in the Emerging and Embedded Business Unit (E^2BU)
• Implementation of "RTL to GDS" processes in 0.15μm, 90nm, and 65nm CMOS technologies.
• Backend Leader of 0.15μm system-on-a-chip (SoC) spin.
• Proficiency in digital implementation tools from Synopsis, Cadence, Magma, Mentor Graphics, and others.

2002–2006
Product Definition Leader.
Puzzle Projects Ltd., Zichron Ya'akov Israel
• Head of product definition, implementation, technical writing and instruction.
• Development of several requirement and definition manuscripts for Command, Control, Communications, Computers and Intelligence (C^4I) systems, including user-interfaces.
• Development of instruction suites for combat systems, including user manuals and instruction courses.
• Course instruction in several countries (USA, Australia, Singapore, Sri Lanka, Israel) in both English and Hebrew as a representative of Rafael.

1994–2001
C^4I Officer.
Naval Branch of the Israeli Defense Forces (IDF)
• Retired with the ranking of Captain, and currently a Major in reserve duty.
• Finished the Israeli Naval Officer's Course (Hovlim) and Advanced Command Course (PIM) with honors.
• Served in operational duty on several classes of naval ships for four years, as a C^4I department officer, deck officer, and patrol boat vice-commander.
• Led the C^4I department of the Naval department of weapons development from 1999-2001, including project definition, development, implementation, and instruction.

Education

2010–2014 | **PhD**, Electronic and Computer Engineering, Ben-Gurion University of the Negev (BGU), Be'er Sheva, Israel.

- Advisor: Dr. Alexander Fish
- Thesis: Low Power Integrated Circuit Arrays (continuation of MSc thesis as part of the combined track to PhD)
- Finished January 2014 with highest regard

2008–2010 | **MSc**, Electronic and Computer Engineering, Ben-Gurion University of the Negev (BGU), Be'er Sheva, Israel.

- Advisor: Prof. Alexander Fish
- Thesis: Low Power Integrated Circuit Arrays
- Thesis grade: 99. Final degree average: 92.9

2002–2006 | **BSc**, Electronic and Computer Engineering, Ben-Gurion University of the Negev (BGU), Be'er Sheva, Israel.

- Finished with honors (GPA 87.03)

Teaching Experience

2014–present	**Advanced Digital VLSI Design 1, BIU** *Graduate-level course* Lecturer: Spring 2014, Spring 2017 • Graduate Course for Nanoelectronics Graduate Degree BIU (∼20 students/year).
2016–present	**Advanced Digital VLSI Design 2, BIU** *Graduate-level course* Lecturer: Spring 2016, Spring 2018 • Graduate Course for Nanoelectronics Graduate Degree BIU (∼20 students/year).
2016–present	**Digital VLSI Design, BIU** *Undergraduate-level 4th year or Graduate-level course* Lecturer: Fall 2016, Fall 2017, Fall 2018 • Mandatory Undergraduate Course for Nanoelectronics Track BIU (∼40 students/year). • Link to course material and recorded lectures: http://www.eng.biu.ac.il/temanad/digital-vlsi-design/
2016–present	**Digital Integrated Circuits, BIU** *Undergraduate-level 3rd-4th year course* Lecturer: Spring 2016, Spring 2017, Spring 2018 • Mandatory Undergraduate Course for Nanoelectronics Track BIU (∼40 students/year). • Link to course material and recorded lectures: http://www.eng.biu.ac.il/temanad/digital-integrated-circuits/
2018–present	**Introduction to Digital Electronic Circuits, BIU.** *Undergraduate-level 3rd year course* Lecturer: Summer 2018 • Mandatory Undergraduate Course at BIU (∼150 students/year). • Link to course material and recorded lectures: http://www.eng.biu.ac.il/temanad/introduction-to-digital-electronic-circuits/
2016–present	**Advanced Nanoelectronics Lab, BIU** *Undergraduate-level 4th year lab* Academic supervisor: Fall 2015, Fall 2016, Fall 2017, Fall 2018 • Graduate Course for Nanoelectronics Graduate Degree BIU (∼15 students/year).
2011–2013	**Introduction to Digital Electronic Circuits, BGU.** *Undergraduate-level 3rd-4th year course* Lecturer: Spring 2011, Spring 2012, Spring 2013, Fall 2013 Teaching Assistant: Fall 2009, Fall 2010, Fall 2011 • Mandatory Undergraduate Course at BGU (250 students/year). • Received the "Teaching Excellence" Award for 2009-10.
2010–2013	**Introduction to VLSI, BGU.** *Undergraduate-level 3rd-4th year course* Lecturer: Spring 2010, Spring 2011, Spring 2012, Spring 2013 Teaching Assistant: Spring 2010 • Track Elective Mandatory Undergraduate Course at BGU (∼90 students/year) • Received the "Teaching Excellence" Award for 2010-11.
2013	**Low Power VLSI, BGU.** *Graduate-level course + lab* Lecturer: Fall 2013 • Complete course development from scratch.
Invited Courses	**Digital Integrated Circuit Design.** *Specialized course for Motorola Solutions* 22.5 hours - Summer 2017

Research Students

PhD Students

- Robert Giterman, PhD student
  Thesis: "*Application-Oriented Alternative Embedded Memories*"
  Graduated Nov. 2018
  (Co-supervisor with Prof. A. Fish)
- Andrea Bonetti, PhD student
  Graduated Dec. 2018
  Thesis: "*Low-Power Design of Digital VLSI Circuits around the Point of First Failure*"
  (Co-advisor with Prof. A. Burg)

MSc Students

Graduated

- Or Maltabashi (*Graduated Jan 2019*)
  Thesis: "*Automatic Guided Physical Implementation of Common Digital Structures*"
- Roman Golman (*Graduated Jan 2019*)
  Thesis: "*Expanding the Usage of GC-eDRAM*"

Started Studies in 2016-17

- Amir Shalom, MSc student (exp. Graduation March 2019)
- Tzachi Noy, MSc student (exp. Graduation July 2019)

Started Studies in 2017-18

- Yosef Lempel, MSc student
  (Co-supervisor with Prof. Y. Shor)
- Daniel Vana, MSc student
  (Co-supervisor with Prof. Y. Shaham, Prof. A. Fish)
- Shani Cohen-Zemach, MSc student

Started Studies in 2018-19

- Yehuda Kra, MSc student
- Odem Harel, MSc student
- Tomer Cohen, MSc student
- Noah Antebi, MSc student
  (Co-supervisor with Prof. Y. Shor)
- Fadi Aboud, MSc student
- Hanan Marinberg, MSc student

(mentored under the supervision of Prof. Andreas Burg)

- Reza Ghanaatian, PhD student
  (Started PhD Studies Sep. 2014)
- Christoph Mueller, PhD student
  (Started PhD Studies May 2015)

(mentored under the supervision of Prof. Alexander Fish)

- Janna Mezhibovsky, MSc student (Graduated Jan. 2012)
  Dynamic Analysis of Low Voltage SRAM Arrays
- Hadar Dagan, MSc student (Graduated Jan. 2013)
  Low Power Non-Volatile Memory for Low-Cost RFID
- Robert Giterman, MSc student (Graduated Sep. 2014)
  Retention Time in Low Power Embedded DRAM Arrays
- Lior Atias, MSc student (Graduated Sep. 2014)
  Robust, Low-Power SRAM for Space Applications

Undergrad. Projects

2018–19
- G. Horden, Y. Greenblatt – *Effective Data Retention Time*
- B. Nevo, N. Ben-Nun – *Guided Physical Implementation of MAC Unit*
- O. Steinberg – *Efficient Level-0 Cache*
- Y. Gindi, D. Ganish – *Hardware Look-up Table for Nonlinear Functions*
- A. Samila, M. Tzfania – *CTRNN implmentation on a eFPGA/X2-DSP partitioned platform*
- D. Shavit – *Custom Cell for Guided Register Files*
- L. Caru, D. Fitouchi – *Simulator for GC-eDRAM*
- E. Zacharov – *Peripherals for GC-eDRAM Array*

2017–18
- A. Yaakov, E. Waserman – *Ternary GC-eDRAM Bitcell*
- O. Harel, Y. Nahum – *Energy-Efficient GC-eDRAM Arrays*
- A. Bernhard, S. Lebel – *Switch Board Management Integration Verification* (with Mellanox)
- N. Maor, A. Guttman – *Guided Placement of AES Block*
- E. Shwartz – *Improved stability of SRAM through Soft Combining*
- O. Eini, O. Yisraeli – *Efficient Manipulation of eFGA in SoC*
- T. Cohen, N. Nahum – *Ensuring 100% Availability for GC-eDRAM Block*

2016–17
- T. Monk – *Thermal Algorithm for Efficient Switch Cooling* (with Dr. Hillel Kluger and Mellanox)
- S. Shtessman, A. Rimer – *Radiation Hardened SRAM in deeply scaled FinFET technologies*
- N. Antebi, B. Turgeman – *Compressors for Wallace Tree Multiplier Arrays*
- A. Mizrachi, R. Mozes – *Generic Fault Injection in Verification IP* (with Mellanox)
- Y. Lempel, Y. Ahrenwald – *Multi-ported Standard Cell Memories*
- H. Marinberg, O. Atash – *Readout circuit for Ternary Gain-Cell*

2015–16
- N. Ozeri – *Ultra Low-leakage SRAM*
- M. Naimer, R. Lupa – *Process Monitoring Feedback Loop*
- C. Grapel – *Low-leakage Pseudo-dynamic Bitcell*

2012–13
- O. Yonah, A. Vaknin – *Low Power SRAM Applications*
- O. Sharon, R. Visotsky – *Dynamic Stability of SRAM Circuits*
- I. Itzin, M. Lieber – *Low Power Gain Cell Embedded DRAM Circuits*

2011-12
- S. Fraiman, N. Adri – *Built in Self-Test Circuit for Data Retention Voltage Operation*
- A. Lazar – *Top-Bottom Gated SRAM for Ultra-Low Power Operation*
- O. Dagan, A. Shamir – *Stacked SRAM for Efficient Energy Conversion*

2010-11
- M. Bar, M. Szekely – *Testing Ultra-Low Power SRAM Circuits*
- A. Tetelbaum, M. Cohen – *Read Before Write SRAM for Low Power Applications*
- O. Rot, S. Pinko – *Analog Circuits for Low Power Non-Volatile Memory*
- A. Serfaty, S. Haviv – *Digital Circuits for Low Power Non-Volatile Memory*

2009-10
- L. Pergament, O. Cohen – *Sub-threshold SRAM Design*
- G. Shveky – *Read Before Write Scheme for Power Reduction in SRAMs*
- T. Azuz – *Optimization of SRAM Architecture According to Density Requirements*

2008-9
- M. Marder, G. Marko – *Low Power Techniques for SRAM Bit Cells*
- T. Yekutiel, A. Postavski – *Power Reduction in Large Array Peripherals*

Professional Memberships

Journal Boards	Elsevier Microelectronics Journal (MEJ), **Editor** – *From 2014*
Conference Technical Committees	ISLPED 2019, **Publicity Chair** – *2019* ICSEE 2018, **Full-Day Symposium Organizer** – *2018* WEEE Workshop, **Steering Board Member**, **Co-Organizer** – *2017* **Assistant Organizer** – *2012, 2015* BIU-imec Networking Event (BINE), **Co-Organizer** – *2016, 2017* CAS Society VLSI Systems and Applications (VSA-TC) **TC Member** – *From 2015* ChipEx Conference, **TC Member** – *2017, 2018* European Workshop on Microelectronics Education (EWME 2018), **PC Member** – *2018* IEEE FTFC conference, **TPF Member** – *2014* IEEE BioCAS Conference, **Committee Member** – *2017* Seiden Workshop, **Session Chair** – *2017* Israeli Microelectronics Olympiad, **Committee Member** – *2013-14*
Professional Societies	IEEE, **Member** – *From 2010* IEEE CAS, **Member** – *From 2012* IEICE, **Member** – *From 2013*
Peer Reviews	IEEE Journal of Solid State Circuits (JSSC) – *From 2011* IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I) – *From 2013* IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II) – *From 2010* IEEE Transactions on VLSI (TVLSI) – *From 2013* IEEE Sensors Journal – From 2011 ACM Transactions on Embedded Computing Systems (TECS) – *From 2015* Elsevier Microelectronics Journal (MEJ) – *From 2012* Elsevier Integration, the VLSI Journal (VLSI-D) – *From 2013* MDPI Journal of Low Power Electronics and Applications (JLPEA) – *From 2010* Springer Journal of Computational Electronics – *From 2015* IEEE International Symposium on Circuits and Systems (ISCAS) – *From 2012* IEEE Biomedical Circuits and Systems Conference (BioCAS) – *From 2013* IEEE Sensors Conference – *From 2009* IEEE Faible Tension Faible Consommation (FTFC) – *From 2014* Asian Symposium on Quality Electronic Design (ASQED) – *From 2012* WSPC Journal of Circuits, Systems, and Computing – *From 2015* Hindawi Journal of VLSI Design – *From 2014* World Scientific Journal of Circuits, Systems, and Computers – *From 2015* IEEE International Conference on the Science of Electrical Engineering (ICSEE) – *From 2016*

Grants, Honors, and Awards

2018–2022 **Israeli Science Fund – Regular Research Program Grant**
- Development of True Approximate Storage for Approximate Computing Applications
- Budget: 270K NIS/year

2018 **Israeli Science Fund – Starting Equipment Grant**
- Laboratory equipment grant for young researchers
- Budget: 2M NIS

2018–2021 **GenPro Consortium, Magnet Program, Israeli Innovation Authority**
- Industry-Academic consortium focusing on RISC-V Ecosystem Development
- Leading research on high-speed Register File Design
- Academic Team Budget: 350K NIS/term
- Co-director of SoC Lab – focal point and integrator of the Consortium

2018–2020 **Magneton**
- "Efficient Implementation of Many Ported Memories for Digital Signal Processing Soft Cores"
- Israeli Innovation Authority program for technology transfer to Israeli industrial partners
- Partnership with CEVA.
- Academic team's budget: 380K NIS/year

2017–2019 **Kamin**
- "High-Density, Low-Power Dynamic FIFO Memories"
- Israeli Innovation Authority program for early technology development
- Budget: 370K NIS/year

2017 **German-Israel Foundation (GIF) - Young Researchers Grant**
- A Comprehensive Architectural Model of Gain-Cell embedded DRAM Memories for System Design and Evaluation

2017 ***Student Awarded*: Katz Scholarship for Research Students in the Sciences**
- Awarded to Mr. Robert Giterman for academic year 2017–2018.

2016 **CDNLive Best Paper Award**
- For the presentation of "FD-SOI Standard cell characterization with Cadence Liberate".

2015–2019 **HiPer Consortium, Magnet Program, Israeli Innovation Authority**
- Industry-Academic consortium focusing on High Performance SoC Design
- Lead research on Gain-Cell embedded DRAM and Efficient Multiplier Design
- Academic Team Budget: 350K NIS/Year
- Co-director of SoC Lab – focal point and integrator of the Consortium

2016–2018 **Erasmus+ "DOCMEN" Project**
- A multi-national project together with Armenia and Kazakhstan, coordinated by Cracow Univ. of Tech. and partnered with ECM Space Tech. GMBH, Politechnico Do Torino, TU Sofia and TU Berlin.

2016 ***Student Awarded*: Lev-Zion Scholarship for Outstanding Doctoral Students**
- Awarded to Mr. Robert Giterman for academic years 2017–2019.

2016 ***Student Awarded*: Ministry of Science, Technology & Space Travel Grant**
- Travel grant to support presentation of PhD work at international conference. Awarded to Mr. Robert Giterman for presentation at ISCAS 2016.

2015 **HiPEAC Paper Award**
- Award for outstanding paper at the Design Automation Conference (DAC).

2014 **Swiss Government Excellence Scholarship for Foreign Students**
- Post-Doctoral fellowship at EPFL during 2014.

2010–2013 **Kreitman Foundation Scholarship**
- Four-year fellowship for PhD Studies from the Kreitman Foundation at BGU.

2013 **Intel Prize**
- Prize presented by Intel for excellence in academic studies and achievement.

2012 **Rector's Prize for Academic Excellence**
• Top award in the Electrical and Computer Engineering Department at BGU.

2012 **Wolf Foundation Prize for Research Excellence**
• National award given out by the Wolf Foundation.

2011–2012 **BGU Outstanding Project Award**
• Prize presented by Ben-Gurion University for project performed outside the required activities of an employee.
• Top prize awarded for developing and implementing the "VLSI Wiki" – a system for information preservation and process enhancement.

2012 **Teaching Excellence Recognition**
• Awarded for the 2010-11 school year by the Electrical and Computer Engineering Department at Ben-Gurion University.

2011 **Teaching Excellence Recognition**
• Awarded for the 2009-10 school year by the Electrical and Computer Engineering Department at Ben-Gurion University.

2010 **Yitzhak Ben Ya'akov HaCohen Excellence Scholarship**
• MSc award from the Yitzhak Ben-Ya'akov HaCohen fund.

Scientific Publications

List of Publications

Books and Book Chapters

B1. P. Meinerzhagen, **A. Teman**, R. Giterman, N. Edri, A. Burg, and A. Fish, *Gain-Cell Embedded DRAMs for Low-Power VLSI Systems-on-Chip*. Springer International Publishing, 2018

Journal Articles

J1. R. Giterman, A. Bonetti, A. Burg, and **A. Teman**, "GC-eDRAM with Body-Bias Compensated Readout and Error Detection in 28nm FD-SOI," *IEEE TCAS-II.*, vol. PP, 2019

J2. R. Giterman, R. Golman, and **A. Teman**, "Improving energy-efficiency in dynamic memories through retention failure detection," *IEEE Access*, vol. PP, 2019

J3. R. Giterman, Y. Weitzman, and **A. Teman**, "Gain-Cell Embedded DRAM Based Physical Unclonable Function," *IEEE Trans. Circuits Syst. I*, vol. 65, pp. 4208–4218, Dec 2018

J4. R. Ghanaatian, A. Balatsoukas-Stimming, C. Muller, M. Meidlinger, G. Matz, **A. Teman**, and A. Burg, "A 588-Gb/s LDPC Decoder Based on Finite-Alphabet Message Passing," *IEEE Trans. VLSI Syst.*, vol. 26, pp. 329–340, Feb 2018

J5. R. Giterman, **A. Teman**, and P. Meinerzhagen, "Hybrid GC-eDRAM/SRAM Bitcell for Robust Low-Power Operation," *IEEE Trans. Circuits Syst. II*, vol. 64, pp. 1362–1366, Dec 2017

J6. A. Bonetti, **A. Teman**, P. Flatresse, and A. Burg, "Multipliers-driven perturbation of coefficients for low-power operation in reconfigurable FIR filters," *IEEE Trans. Circuits Syst. I*, vol. 64, pp. 2388–2400, Sept 2017

J7. A. Bonetti, N. Preyss, **A. Teman**, and A. Burg, "Automated integration of dual-edge clocking for low-power operation in nanometer nodes," *ACM Trans. on Design Automation of Elec. Systems*, vol. 22, pp. 62:1–62:20, May 2017

J8. D. Rossi, A. Pullini, I. Loi, M. Gautschi, F. Kagan Gurkaynak, **A. Teman**, J. Constantin, A. Burg, I. Miro-Panades, E. Beigné, F. Clermidy, F. Abouzeid, P. Flatresse, and L. Benini, "Energy-Efficient Near-Threshold Parallel Computing: The PULPv2 Cluster," *IEEE Micro.*, vol. 37, pp. 20–31, September 2017

J9. R. Giterman, L. Atias, and **A. Teman**, "Area and energy-efficient complementary dual-modular redundancy dynamic memory for space applications," *IEEE Trans. VLSI Syst.*, vol. 25, pp. 502–509, Feb 2017

J10. R. Giterman, A. Fish, N. Geuli, E. Mentovich, A. Burg, and **A. Teman**, "An 800MHz Mixed-VT 4T IFGC Embedded DRAM in 28nm CMOS Bulk Process for Approximate Storage Applications," *IEEE J. Solid-State Circuits*, vol. 53, pp. 2136–2148, July 2018

J11. R. Giterman, A. Fish, A. Burg, and **A. Teman**, "A 4-Transistor nMOS-Only Logic-Compatible Gain-Cell Embedded DRAM With Over 1.6-ms Retention Time at 700 mV in 28-nm FD-SOI," *IEEE Trans. Circuits Syst. I*, vol. 65, pp. 1245–1256, April 2018

J12. A. Kazimirsky, **A. Teman**, N. Edri, and A. Fish, "An 0.65 V 500 MHz integrated dynamic and static RAM (iD-SRAM) for video applications," *IEEE Trans. VLSI Syst.*, vol. 25, no. 9, pp. 2411–2418, 2017

J13. L. Moyal, I. Levi, **A. Teman**, and A. Fish, "Synthesis of dual mode logic," *Integration the VLSI Journal.*, vol. 55, pp. 246–253, 2016

J14. **A. Teman**, D. Rossi, P. Meinerzhagen, L. Benini, and A. Burg, "Power, area, and performance optimization of standard cell memory arrays through controlled placement," *ACM Trans. on Design Automation of Elec. Systems*, vol. 21, pp. 59:1–59:25, May 2016

J15. L. Atias, **A. Teman**, R. Giterman, P. Meinerzhagen, and A. Fish, "A low-voltage 13T radiation hardened SRAM bitcell for low-voltage operation," *IEEE Trans. VLSI Syst.*, vol. 24, no. 8, pp. 2622–2633, 2016

J16. N. Edri, P. Meinerzhagen, **A. Teman**, A. Burg, and A. Fish, "Silicon-proven per-cell retention time distribution model of gain-cell based eDRAM," *IEEE Trans. Circuits Syst. I*, vol. 63, pp. 222–232, Feb 2016

J17. R. Giterman, **A. Teman**, P. Meinerzhagen, L. Atias, A. Burg, and A. Fish, "Single-supply 3T gain-cell for low-voltage low-power applications," *IEEE Trans. VLSI Syst.*, vol. 24, no. 1, pp. 358–362, 2016

J18. **A. Teman** and R. Visotsky, "A fast modular method for true variation-aware separatrix tracing in nanoscaled SRAMs," *IEEE Trans. VLSI Syst.*, vol. 23, no. 10, pp. 2034–2042, 2015

J19. H. Dagan, A. Shapira, **A. Teman**, A. Mordakhay, S. Jameson, E. Pikhay, V. Dayan, Y. Roizin, E. Socher, and A. Fish, "A low-power low-cost 24 GHz RFID tag with a C-Flash based embedded memory," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1942–1957, 2014

J20. **A. Teman**, P. Meinerzhagen, R. Giterman, A. Fish, and A. Burg, "Replica technique for adaptive refresh timing of gain-cell-embedded DRAM," *IEEE Trans. Circuits Syst. II*, vol. 61, no. 4, pp. 259–263, 2014

J21. P. Meinerzhagen, **A. Teman**, A. Fish, and A. Burg, "Impact of body biasing on the retention time of gain-cell memories," *The Journal of Engineering*, vol. 1, no. 1, 2013

J22. P. Meinerzhagen, **A. Teman**, R. Giterman, A. Burg, and A. Fish, "Exploration of sub-VT and near-VT 2T gain-cell memories for ultra-low power applications under technology scaling," *MDPI J. Low Power Elec. and App.*, vol. 3, no. 2, pp. 54–72, 2013

J23. H. Dagan, **A. Teman**, E. Pikhay, V. Dayan, A. Mordakhay, Y. Roizin, and A. Fish, "A low-power DCVSL-like GIDL-free voltage driver for low-cost RFID nonvolatile memory," *IEEE J. Solid-State Circuits*, vol. 4, no. 6, pp. 1497–1510, 2013

J24. **A. Teman**, A. Mordakhay, and A. Fish, "Functionality and stability analysis of a 400 mV quasi-static RAM (QSRAM) bitcell," *Microelectronics Journal*, vol. 44, no. 3, pp. 236–247, 2013

J25. **A. Teman**, H. Dagan, V. Dayan, E. Pikhay, Y. Roizin, and A. Fish, "Zero-cost ultra-low power non-volatile memory module for RFID applications," *TowerJazz Technical Journal*, vol. 4, pp. 46–49, July 2013

J26. A. Spivak, **A. Teman**, A. Belenky, O. Yadid-Pecht, and A. Fish, "Low-voltage 96 dB snapshot CMOS image sensor with 4.5 nW power dissipation per pixel," *MDPI Sensors*, vol. 12, no. 8, pp. 10067–10085, 2012

J27. **A. Teman**, O. Yadid-Pecht, and A. Fish, "Leakage reduction in advanced image sensors using an improved AB^2C scheme," *IEEE Sensors J.*, vol. 12, no. 4, pp. 773–784, 2012

J28. **A. Teman**, A. Mordakhay, J. Mezhibovsky, and A. Fish, "A 40-nm sub-threshold 5T SRAM bit cell with improved read and write stability," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 12, pp. 873–877, 2012

J29. A. Spivak, **A. Teman**, A. Belenky, O. Yadid-Pecht, and A. Fish, "Power-performance tradeoffs in wide dynamic range image sensors with multiple reset approach," *MDPI J. Low Power Elec. and App.*, vol. 1, no. 1, pp. 59–76, 2011

J30. **A. Teman**, L. Pergament, O. Cohen, and A. Fish, "A minimum leakage quasi-static RAM bitcell," *MDPI J. Low Power Elec. and App.*, vol. 1, no. 1, pp. 204–218, 2011

J31. **A. Teman**, L. Pergament, O. Cohen, and A. Fish, "A 250 mV 8 kb 40 nm ultra-low power 9T supply feedback SRAM (SF-SRAM)," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2713–2726, 2011

J32. **A. Teman**, O. Yadid-Pecht, and A. Fish, "Large VLSI arrays – power and architectural perspectives," *International Journal of Information Technologies and Knowledge (IJ ITK)*, vol. 4, no. 1, pp. 76–90, 2010

Peer-reviewed Conference Proceedings

C1. T. Monk, H. Kugler, O. Maori, and **A. Teman**, "TEMPO: Thermal-Efficient Management of Power in High-Throughput Network Switches," in *Accepted to VLSI-DAT 2019*, 2019

C2. O. Maltabashi, H. Marinberg, R. Giterman, and **A. Teman**, "A 5-Transistor Ternary Gain-Cell eDRAM with Parallel Sensing," in *Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018

C3. A. Bonetti, J. Constantin, **A. Teman**, and A. Burg, "A Timing-Monitoring Sequential for Forward and Backward Error-Detection in 28 nm FD-SOI," in *Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 2018

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C17. R. Ghanaatian, P. Whatmough, J. Constantin, **A. Teman**, and A. Burg, "A low-power correlator for wake-up receivers with algorithm pruning through early termination," in *Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 2667–2670, May 2016

C18. R. Giterman, **A. Teman**, L. Atias, and A. Fish, "A soft error tolerant 4T gain-cell featuring a parity column for ultra-low power applications," in *Proc. of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1–2, October 2015

C19. S. Ganapathy, G. Karakonstantis, **A. Teman**, and A. Burg, "Mitigating the impact of faults in unreliable memories for error-resilient applications," in *Proc. of the Design Automation Conference (DAC)*, DAC '15, (New York, NY, USA), pp. 102:1–102:6, ACM, 2015 **(Conference acceptance rate: 20%.)** *Recipient of HiPEAC Paper Award 2015.*

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C23. **A. Teman**, D. Rossi, P. Meinerzhagen, L. Benini, and A. Burg, "Controlled placement of standard cell memory arrays for high density and low power in 28nm FD-SOI," in *Proc. of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 81–86, IEEE, 2015 **(Conference acceptance rate: 33%.)**

C24. L. Atias, **A. Teman**, and A. Fish, "Single event upset mitigation in low power SRAM design," in *Proc. of IEEE Conv. of Electrical and Electronics Eng. in Israel (IEEEI)*, pp. 1–5, IEEE, 2014

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C27. A. Vaknin, O. Yona, and **A. Teman**, "A double-feedback 8T SRAM bitcell for low-voltage low-leakage operation," in *Proc. of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1–2, IEEE, 2013

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C31. P. Meinerzhagen, **A. Teman**, A. Mordakhay, A. Burg, and A. Fish, "A sub-VT 2T gain-cell memory for biomedical applications," in *Proc. of IEEE Subthreshold Microelectronics Conference (SubVT)*, pp. 1–3, IEEE, 2012

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C38. **A. Teman**, O. Yadid-Pecht, and A. Fish, "An improved AB^2C scheme for leakage power reduction in image sensors with on-chip memory," in *Proc. of IEEE Sensors*, pp. 193–196, IEEE, 2009

C39. S. Fisher, **A. Teman**, D. Vaysman, A. Gertsman, O. Yadid-Pecht, and A. Fish, "Ultra-low power subthreshold flip-flop design," in *Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 1573–1576, IEEE, 2009

C40. S. Fisher, **A. Teman**, D. Vaysman, A. Gertsman, O. Yadid-Pecht, and A. Fish, "Digital subthreshold logic design-motivation and challenges," in *Proc. of IEEE Conv. of Electrical and Electronics Eng. in Israel (IEEEI)*, pp. 702–706, IEEE, 2008

C41. **A. Teman**, S. Fisher, L. Sudakov, A. Fish, and O. Y. Pecht, "Autonomous CMOS image sensor for real time target detection and tracking," in *Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 2138–2141, IEEE, 2008

In review or final stages of preparation

S1. A. Bonetti, R. Golman, R. Giterman, **A. Teman**, and A. Burg, "Gain-Cell Embedded DRAMs: Modeling and Design Space," *Under final stages of review in IEEE TVLSI.*, 2019

S2. O. Maltabashi, Y. Kra, and **A. Teman**, "A physical-aware clustering approach for fused dot-product implementation," *Under final stages of review in IEEE TCAD.*, 2019

S3. D. Vana, P.-E. Gaillardon, and **A. Teman**, "C^2MOS design with Three-Independent-Gate Field Effect Transistors," *Submitted to IEEE TCAS-I.*, 2019

Patents

P1. O. Maltabashi, Y. Kra, and **A. Teman**, "Physically-aware affinity-driven multiplier implementation," 2018. US Provisional App. 62/775909

P2. T. Noy and **A. Teman**, "Embedded DRAM based FIFOs," 2018. US Provisional App. 16199448

P3. R. Giterman, Y. Weizman, and **A. Teman**, "Dynamic memory physical unclonable function," 2018. US Provisional App. 62662303

P4. R. Giterman, , A. Fish, **A. Teman**, *et al.*, "High density memory macro," 2017. US Patent App. 62/555,107

P5. R. Giterman, L. Atias, A. Fish, and **A. Teman**, "Complementary dual modular redundancy memory cell," 2016

P6. R. Giterman, **A. Teman**, P. Meinerzhagen, A. Burg, and A. Fish, "Transistor gain cell with feedback," June 27 2017. US Patent 9,691,445

P7. **A. Teman**, L. Pergament, O. Cohen, and A. Fish, "Ultra low power memory cell with a supply feedback loop configured for minimal leakage operation," July 4 2013. US Patent 20,120,281,459, 2,012

P8. **A. Teman**, L. Pergament, O. Cohen, and A. Fish, "Ultra low power SRAM cell circuit with a supply feedback loop for near and sub threshold operation," Nov. 8 2012. US Patent 20,120,281,458

Competitive Peer-Reviewed Lectures and Posters not followed by a publication

L1. O. Maltabashi and **A. Teman**, "Efficient Implementation of Latch-based Standard Cell Memory arrays in 28nm CMOS," in *IEEE ICSEE, Special session on Advanced Topics in Nanoscaled Integrated Circuits and Systems*, November 2016

L2. R. Golman, R. Giterman, and **A. Teman**, "Scaling Gain-Cell embedded DRAM to Advanced Nodes," in *Seiden Workshop – Beyond CMOS: From Devices to Systems*, June 2017

L3. **A. Teman**, A. Bonetti, C. Mueller, and A. Burg, "FD-SOI Standard cell characterization with Cadence Liberate," in *CDNLive Israel*, September 2016 *Awarded Best Paper CDNLive Israel 2016.*

L4. O. Maltabashi and **A. Teman**, "Controlled Placement of Standard Cell Memory Arrays," in *IEEE Israel Conference of Students and Young Professionals*, June 2016

L5. A. Shalom, R. Golman, R. Giterman, and **A. Teman**, "A Comprehensive Model for the Architectural Design of Gain-Cell embedded DRAM Based Memories," in *IEEE Israel Conference of Students and Young Professionals*, June 2016

L6. A. Bonetti, N. Preyss, A. Burg, and **A. Teman**, "Dual-edge triggered clocking - how we can use it and when," in *CDNLive Israel*, October 2015

L7. A. Bonetti, N. Preyss, **A. Teman**, and A. Burg, "Physical implementation of dual-edge clocking - a seamless mixed-integration methodology," in *CDNLive EDMA*, April 2015

L8. A. Bonetti, J. Constantin, **A. Teman**, and A. Burg, "Circuits and techniques for dynamic timing monitoring in microprocessors," in *Nanotera Annual Meeting 2015*, May 2015

L9. **A. Teman**, G. Karakonstatis, S. Ganapathy, and A. Burg, "Exploiting application error resilience for energy savings in memories," in *Workshop on Approximate Computing (WAPCO)*, January 2015

L10. **A. Teman** and A. Fish, "SRAM stability in the nanoscale era," in *CDNLive Israel*, September 2012

L11. **A. Teman** and A. Fish, "Low voltage logic and SRAM design," in *ChipEx 2011*, May 2011

Organization of Special Sessions, Events, Workshops

W1. "Symposium on Circuits and Systems," Special Symposium at IEEE ICSEE 2018, Nov, 2018, Eilat, Israel.

W2. "Workshop on Energy-Efficient Electronics (WEEE) 2017," Workshop held in Ystad, Sweden, June, 2017.

W3. "Bar Ilan–imec Networking Event 2017," Event held at Bar-Ilan University, March, 2017, Ramat Gan, Israel.

W4. "Advanced Topics in Nanoscaled Integrated Circuits and Systems," Workshop at IEEE ICSEE 2016, Nov, 2016, Eilat, Israel.

W5. "Bar Ilan–imec Networking Event," Event held at Bar-Ilan University, March, 2016, Ramat Gan, Israel.

W6. "Dependable and Energy Efficient SoC Design in Scaled Technologies," Special Session at IEEE Israel 2014, Nov, 2014, Eilat, Israel.

Invited Talks and Lectures

T1. "Dynamic Stability and Noise Margins of SRAM Arrays in Nanoscaled Technologies," IEEE FTFC 2014, May, 2014, Monte Carlo, Monaco .

T2. "Embedded Memory Design Challenges in the NanoScale Era," Mellanox, 2013, Yokneam, Israel.

T3. "Embedded Memory Design Challenges in the NanoScale Era," IBM, 2013, Tel Aviv, Israel.

T4. "Low Power Integrated Circuit Array Design," Tel Aviv University, 2012, Tel Aviv, Israel .

T5. "Low Power Integrated Circuit Array Design," Bar Ilan University, 2012, Ramat Gan, Israel.

T6. "Internal Feedback Sub-Threshold SRAM Bitcells," Alpha Consortium final conference, 2011, Tel Aviv, Israel.

T7. "Low voltage Logic and SRAM design," Zoran Corporation, 2011, Haifa, Israel.

T8. "Low voltage Logic and SRAM design," IBM, 2011, Tel Aviv, Israel.

T9. "An Improved AB^2C for Leakage Reduction in Smart Image Sensors," Ben Gurion University, 2010, Be'er Sheva, Israel.

Research Tapeouts (Fabricated Test Chips)

SoC2 2019	System-on-Chip in 16 nm FinFET • Technology: TSMC 16FFC • Flagship project of HiPer Consortium. • Co-academic director and leader of GC-eDRAM block.
Kwak 2018	Embedded DRAM Test Chip in 28 nm FD-SOI • Technology: Samsung 28nm FD-SOI • Joint design with EPFL. • Project director.
Martini 2017	Embedded DRAM Test Chip in 28 nm FD-SOI • Technology: ST 28nm FD-SOI • Joint design with EPFL. • Project leader.
BEER 2017	Embedded DRAM Test Chip in 28 nm FD-SOI • Technology: ST 28nm FD-SOI • Joint design with EPFL. • Project leader.
DAFNA 2016	Embedded DRAM Test Chip in 28 nm Bulk • Technology: TSMC 28nm HPM • Joint design with Mellanox. • Project leader.
Polar Bear 2015	Polar Decoder chip • Technology: ST 28nm FD-SOI • Joint venture between EPFL and McGill University. • Management of physical implementation of chip.
PULP-III 2015	Flexible multi-core platform for energy efficient computing • Technology: ST 28nm FD-SOI • Participant in large, multi-partner project with ST-Microelectronics, UNIBO, ETH-Zurich, and CEA-Leti. • Participant in architecture, design, and planning of body-bias generation block.
dynOR 2015	Scalable CPU with early-edge detection and clock generation unit • Technology: ST 28nm FD-SOI • Project leader and head engineer.
CAMEL 2014	Memory and cryptography test chip Techonology: TSMC 65nm LP • Advisor for design and physical implementation of multi-project test chip with Bar-Ilan University.
DDFSE 2014	60GHz wi-fi test chip • Technology: TSMC 40nm LP • Advisor for physical implementation of 2 Million gate, very complex hard macro.
PULP-II 2014	Flexible multi-core platform for energy efficient computing • Technology: ST 28nm FD-SOI • Participant in large, multi-partner project with ST-Microelectronics, UNIBO, and ETH-Zurich. • In charge of Standard Cell Memory block design and integration and special cell characterization and integration.
GREENBELT2 2013	Gain-cell embedded DRAM and SRAM for space applications test chip • Technology: UMC 0.18μm • Led project, designed all included components, and carried out tape-out procedure, in collaboration with EPFL.
GREENBELT 2012	Gain-cell embedded DRAM test chip • Technology: UMC 0.18μm • Led project, designed all included components, and carried out tape-out procedure, in collaboration with EPFL.

RFID 2010–2012	Single Chip RFID Demonstrator in standard CMOS process • Technology: TowerJazz 0.18μm • Participated in the design, tape-out procedures and measurements of 10 test-chips, as part of a multi-year project. • Project culminated with a fully operational low-cost low-power RFID Demonstrator. • Cooperation with Tel Aviv University and Tower Semiconductor.
RAMBO 2010	Subthreshold SRAM test chip. • Technology: TSMC 40nm LP • Led project, designed all included components, carried out tape-out procedure and measurements. • First 40 nm test chip by an academic group in Israel. • Cooperation with Zoran in tape-out procedure.
Sub-Vt 2008	Subthreshold logic test chip including AB^2C smart imager • Technology: TSMC 80nm • Responsible for several of the included test circuits and components. • Led full-chip integration and tape-out. Participated in measurements. • Cooperation with Zoran in tape-out procedure.