Photonic XOR with inherent loss compensation mechanism for memory cell implementation in a standard nanoscale very large-scale integrated fabrication process

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A multilayer photonic XOR gate is presented. The XOR is implemented by the interconnect layers of a microelectronic chip and is suitable for fabrication in a standard VLSI fabrication process. The proposed device features an inherent insertion loss compensation mechanism by utilization of nanometric holes, making it possible to implement an optic memory cell without the need of additional complex compensation devices. The structure of such a memory cell, implemented by utilization of two proposed XOR gates, configured to perform the NOT function, is shown. The unique structure of the proposed device allows us to significantly reduce sensitivity to process variations and therefore makes it possible to utilize the memory cell in state-of-the-art nanoscale processes. The proposed memory can be integrated with conventional electronics on the same VLSI chip. © 2013 Optical Society of America

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Since the introduction of Moore’s law in 1965 [1], which predicted that the number of transistors on a chip will double approximately every two years, the microelectronics industry has faced many challenges. On one hand, many efforts have been made to develop small and fast devices, which achieve high reliability with aggressive technology scaling [2]. However, the speed and reliability of electronic devices are limited by electronic interference and the low mobility of electrons. On the other hand, with advancements in technology and continuous process scaling, power dissipation of VLSI chips has become one of the fundamental limits in both high-performance microprocessors and low- to medium- performance portable systems [3]. Finally, the requirement to integrate a variety of functions, such as digital and analog computation, memories, sensing, and interconnect in a single VLSI system, has recently resulted in attempts to develop More-than-Moore approaches, such as 3D VLSI [4].

Recently, electro-optical and all-optical devices have been proposed as an alternative to conventional transistors and logic gates [5–7]. The advantages of optical devices over conventional electronics include relative immunity to electronic interference, high SNR, high bandwidth, and low channel crosstalk.

In this Letter we present a novel (to our knowledge) photonic XOR device with an inherent loss compensation mechanism. The proposed device is suitable for fabrication in a standard CMOS nanoscaled process, and it can be implemented using the existing interconnect layers of a VLSI chip. Therefore, both electronic and optical computation (logic and memory) can be implemented and integrated on the same chip without affecting each other while saving area by using layers in the chip that are unused today. This approach allows us to relax the size requirements of the optical device, a common drawback in current silicon photonics research. The aforementioned features of the proposed XOR, in addition to reduced sensitivity to process variations in state-of-the-art nanoscale processes, make it an ideal choice for a memory cell implementation. This memory can be used as a basic building block for static random memory (SRAM), dynamic random memory (DRAM), temporary memory buffer, digital latch, and flip–flop implementations.

Figure 1(a) shows the structure of the proposed XOR gate (without the compensation mechanism). The gate consists of three waveguides, separated by two thick metal layers. Two waveguides serves as inputs to the gate [marked as A and B in Fig. 1(a)], while one of the waveguides functions as the gate output [marked as Output in Fig. 1(a)].

The gate makes use of materials that are standard in a conventional VLSI process, i.e., silicon dioxide (SiO₂), with a refractive index of \( n = 1.48 \), and copper (Cu), with a refractive index of \( N = 0.606 - j8.26 \) [8], for waveguide and metal implementations, respectively. The dimensions of the device are as follows: the input waveguides are 610 nm wide, the output waveguide has a width of 800 nm, the thickness of the metal layers is 30 nm, and the length of the device is 14.7 \( \mu \)m. Note that as predicted by the International Technology Roadmap for Semiconductors (ITRS) [9], the metal pitch in a standard fabrication process will reach 30 nm in 2014. The light wavelength of 1.55 \( \mu \)m, which is standard in optical communications, was assumed in the device design.

![Fig. 1. Proposed photonic circuit: (a) the XOR gate (without compensation mechanism) and (b) the proposed memory cell. Eref is used to transform the XOR operation into a NOT operation for the memory cell implementation.](http://dx.doi.org/10.1364/OL.38.001473)
The device relies on the coupled mode theory \[10\], an effect that occurs between each two waveguides and causes an interaction between them. The metal between the waveguides accumulates phase difference, which depends on the length of the metal. The light propagates through the waveguides and interferes at the end of the device according to the relative phase between waveguides. The length of the device is set such that a phase difference of \( \pi \) is accumulated between waveguides, thus creating the amplitude modulated XOR logic function, as can be seen in Figs. 2(a) and 2(b). When two signals are received at both inputs A and B, a destructive interference occurs due to different phase accumulation along the waveguides and therefore energy does not build up at the output, as shown in Fig. 2(c).

It can be clearly seen that if signals with high amplitude are considered as “1” and signals with low amplitude are considered as “0,” the proposed device implements the XOR logical gate. Table 1 shows an example of the gate operation with input signals having a 1 \( \text{V/m} \) amplitude. The calculated extinction ratio (for the above specification) is 23.977 dB.

A number of simulations have been carried out to examine the robustness of the proposed device to process variations. The device was examined for variations in the parameters, such as waveguide width, length of the device, and metal width. An asymmetric change in the metal width, for example, can indicate sustainability of the gate to inputs with asynchronous phases.

Figure 3(a) depicts the extinction ratio in the presence of variations in the size of the internal waveguide (input A) for different gate lengths, and Fig. 3(b) presents the insertion loss under the same variation. As can be seen, the variations in device length have a limited influence on the extinction ratio and on the insertion loss. Conversely, the variations in internal waveguide width have an increased influence on the extinction ratio and on the insertion loss.

The influence of asymmetric variations in the metal thickness and external waveguide variation is shown in Figs. 4 and 5, respectively. Under these variations the device behavior is more robust. For different metal sizes there is a slight change in the insertion loss. Also, the extinction ratio has some degradation, but it is still high enough for the logic operation. The sensitivity of the device to external waveguide variations is very similar to the sensitivity to metal variations.

The device simulations show that its extinction ratio can stand the following process variations: variations in input A of \( \pm 2.5\% \), in input B of \( \pm 2.5\% \), in the third waveguide of \( \approx -6.5\% \) and more than \(+10\% \), and in the metal thickness of \( \pm 10 \text{ nm} \), assuming extinction ratio degradation of up to 2 dB. Although most of the fabrications facilities (fabs) keep the process variation data confidential, the acceptable numbers for a conservative evaluation of 3\( \sigma \) are 7.5\%–10\% \[11\]. As can be seen, our device achieves high robustness, and in many cases it has good endurance even to these conservative variations.

In order to cascade two such logic gates, one has to overcome the insertion losses in each stage. This requires a compensation mechanism that relies on the coupling of an optical signal to surface plasmons. Here we use nanometric holes that are generated in the upper metal layer and an additional reference beam (denoted as the gain beam) that is injected through the upper oxide layer, appearing in Fig. 1(a). The photons of the gain beam injected into the upper oxide layer are converted to surface plasmons, and their interaction with input beam A around the small holes generates gain due to the surface-enhanced plasmon resonance effect. Thus, the energy of the gain beam injected into the upper oxide layer is converted into plasmons, and they are converted into photons of input A. As a result they amplify the photons of beam A through the interaction of beam A with the nanoholes made in the upper metal layer. The process can be described by the following equation:

\[
P_{\text{out}} = \eta C_{\text{abs}} I_{\text{gain}}.
\]

where \( P_{\text{out}} \) is the amplified signal power output, \( \eta \) is the quantum efficiency of the process, \( C_{\text{abs}} \) is the absorption cross section of the holes, and \( I_{\text{gain}} \) is the intensity of the gain beam. This gain compensates the optical losses involving the propagation through the waveguide of Fig. 1(a) and will also allow the usage of the configuration of Fig. 1(a) as part of an optical memory device, as described below.

The holes can be made as an array of holes, while the fabrication process can involve fabricating a 2D net of lines in the upper metal layer where the distance between two adjacent lines in the net is only a few nanometers.

### Table 1. Photonic Gate Logic Operation

<table>
<thead>
<tr>
<th>Power [nW/m]</th>
<th>Logic Value</th>
<th>Power [nW/m]</th>
<th>Logic Value</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1.57</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.196</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1.197</td>
<td>1</td>
<td>0.191</td>
</tr>
<tr>
<td>1.57</td>
<td>1</td>
<td>1.197</td>
<td>1</td>
<td>4.8e – 4</td>
</tr>
</tbody>
</table>
The gain is obtained through the generation of higher harmonics in the gain layer. The pump beam with frequency \( \omega_p \) gives rise to higher harmonic light with frequency \( \omega_n \), which is the same as that of the signal. This higher harmonic light is a result of the physical confinement of oscillating electrons in the metallic structures [12]. The higher harmonic light then interferes with the signal to generate a field with an intensity that is proportional to \( E_1^2 E_2 \), where \( E_1 \) is the signal and \( E_2 \) is the generated higher harmonic field. The pump beam is filtered out by the waveguide dimensions and does not propagate to the output. In order to filter out the \( |E_1|^2 \) term, we illuminate at an angle from the two opposite directions of the waveguide. Thus, the \( |E_1|^2 \) will be a standing wave with no k vector component in the direction of the waveguide. The exact design of the gain structures is beyond the scope of this work and is the subject of a subsequent publication. Assuming that \( E_2 > E_1 \), the gain at each gain site (i.e., the physical confinement site where the higher harmonic is generated) in terms of optical power is \( 2E_2^2/E_1 \), and for \( N \) such gain sites it is \( 2NE_2^2/E_1 \).

An example of a basic memory cell employing the proposed XOR gate is shown in Fig. 1(b). The memory consists of two XOR gates, which are configured to perform the NOT function. This is done by connecting the input B to a fixed reference and using input A as the logic input. The two gates are cascaded in such way that the input of one gate is connected to the output of the second one, creating a memory cell (the connection between the output of one of the gates to the input of the second one is made through a 3 dB coupler that allows some of the signal to be read at the output of the memory cell). The bending of the light beam is obtained by a method presented in [13] for the initial examination. The adaptation to the standard fabrication process is obtained by a micromirror instead of light bending by a photonic-crystal-like structure.

The phase at the output of each of the XOR gates depends on the input waveguide. While the input into one waveguide results in an amplitude of logical “1” with zero phase, an input of “1” to the other waveguide will result in an output with the same amplitude but a phase of \( \pi \) [14]. This situation does not allow for cascading of the two XOR gates in order to construct the memory cell and can be rectified by phase encoding the input signals. In this solution, random intrabit phase encoding is applied, where the phase of each intrabit at the input of the device is either 0 or \( \pi \). At the output the decision between logical “1” or “0” is determined by setting a threshold. If the ratio of the intrabits with an amplitude of logical “0” is larger than the threshold, the corresponding bit is determined to be “0”; otherwise, the bit is determined to be “1.” This solution allows for the cascading of multiple XOR gates with a relatively low bit error rate [15].

Since the proposed XOR device is used as a core of this memory cell, the memory cell is also suitable for fabrication in a standard process, presenting a reduced sensitivity to process variations. This makes it possible to utilize the memory cell as a basic building block for SRAM, DRAM, temporary memory buffer, digital latch, and flip–flop implementations in many practical applications. One should note that the losses within the memory cell due to the coupling of the signal to the output of the cell (through the 3 dB coupler) can be compensated by the same aforementioned compensation mechanism.

References

15. A. Meiri and Z. Zalevsky are preparing a paper titled “Cascading of all-optical devices with arbitrary phase output by intra-bit phase encoding.”