Global Shutter CMOS Image Sensor With Wide Dynamic Range

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Abstract — A novel concept for global shutter CMOS image sensors with Wide Dynamic Range (WDR) implementation is presented. The proposed imager is based on the multisampling WDR approach and it allows an efficient global shutter pixel implementation achieving small pixel size and high fill factor. The proposed imager provides wide DR by applying adaptive exposure time to each pixel, according to the local illumination intensity level. Two pixel configurations, employing different kinds of a 1-bit in-pixel memory were implemented. An imager, including two different pixels was designed and simulated in 0.18µm CMOS technology. System architecture and operation are discussed and simulation results are presented.

Index Terms—Active Pixel Sensor (APS), Wide Dynamic Range (WDR), Global Shutter Imager.

I. INTRODUCTION

Driven by the demand for low-power dissipation in state-of-the-art portable image systems, CMOS imagers became very attractive. CMOS imagers offer significant advantages in terms of low-power, low-voltage and monolithic integration, rivaling traditional CCDs [1]-[4]. Sensor Dynamic Range (DR) is one of the most important figures of merit in state of the art CMOS image sensors. The DR problem exists in cases where the sensor should capture scenes having a wide range of illumination. Bright scenes and wide variations in intrascene illumination can arise in many situations: driving at night, photographing people in front of a window, observing an aircraft landing at night, and imaging objects for studies in meteorology or astronomy.

Generally, dynamic range can be increased in two ways: the first one is noise reduction and thus expanding the dynamic range toward darker scenes. The second method is incident light saturation level expansion, thus improving the dynamic range toward brighter scenes. In this paper, the last approach is discussed. A narrow DR of image sensors entails saturation of a pixel with high sensitivity, in a case of high illumination levels, and part of the information can be lost. DR insufficiency of conventional video cameras is a serious problem in realizing a robust vision system for taking images consisting of varying illumination conditions in the same scene.

Different solutions for widening the DR in CMOS image sensors have been presented in recent years [5]-[16].

This paper presents a novel implementation of a wide DR (WDR) CMOS image sensor. The proposed imager operates both in global and rolling shutter modes of operation and achieves very high dynamic range expansion of up to 120dB. This implementation is a continuation of our previous work, where we have implemented an ultra low-power WDR sensor, operating in the global shutter mode [12]. However, a number of significant improvements differ this newly proposed sensor architecture from our previous solution. The main advantage of the presented imager is a simpler design, increased fill factor, lower FPN and therefore better image quality and improved spatial resolution. All these improvements were allowed by implementation of a 1-bit in-pixel memory and performing most of the required processing for DR expansion in the array periphery, while still allowing global shutter operation. Two pixel configurations, employing different kinds of a 1-bit in pixel memory are shown here.

Section II describes the system architecture, system building blocks and briefly presents the WDR algorithm. Section III depicts the pixel structure implementations and the general principle of operation. Section IV discusses simulation results. Conclusions and future research are outlined in Section V.

II. SYSTEM ARCHITECTURE AND WDR ALGORITHM DESCRIPTION

Figure 1 shows the general architecture of the proposed imager using the designed prototype photograph as a template. The sensor consists of a pixel array, one row (vertical) decoder, two column (horizontal) decoders, column readout circuits, processing circuits and digital memory. In order to share the processing circuits among the pixels in a column, the design makes use of a column parallel architecture. In this architecture, the pixel array, the memory array, and the processing elements are separated. Each pixel contains a 1-bit memory cell that allows the possibility of independent reset of each pixel. With this, the adjustability of integration time can be performed for each pixel, and nondestructive readout of the pixel can be performed at any time during the integration period.

The processing element contains the saturation detection circuitry that is shared by all pixels in a column. Because of this column parallel architecture, the pixel array contains a minimum amount of additional circuitry and there is a little sacrifice in fill factor in comparison with previous snapshot designs.

A. WDR Algorithm Description

The design of the imager is based on our previously proposed WDR algorithm [10], which was adapted here to allow an efficient global shutter sensor implementation. According to our algorithm, the required expansion of the DR is determined by a series of $W$ bits. The total integration time is subdivided into several integration times, which are progressively shorter, according to the down-going series:

$$T_{\text{int}}/X^1, T_{\text{int}}/X^2, ..., T_{\text{int}}/X^W \quad (1)$$
where $X > 1$ and $T_{\text{INT}}$ represents the full integration time.

At the beginning of the frame, all pixels in the imager are reset simultaneously to ensure snap-shot operation of the imager. Then the photodiode output of each pixel in row $k$ is compared with an appropriate threshold, at certain time points given by:

$$T_{\text{INT}} \cdot \left( T_{\text{INT}} / X^{i} \right) - \Delta t_{k}, \ldots, T_{\text{INT}} \cdot \left( T_{\text{INT}} / X^{m} \right) - \Delta t_{k}$$

(2)

where $\Delta t_{k}$ is a short time associated with row $k$ and given as:

$$\Delta t_{k} = (N - k + 1) \cdot T_{\text{decision}}$$

(3)

where $T_{\text{decision}}$ is the decision time and will be described later on. The comparison is performed by enabling the column shared comparator with constant threshold value $V_{\text{th}, i}$ to all pixels in the array, in a row-by-row manner, i.e. each comparator with a single pixel in a row, applied to all rows, one at a time. The comparison checks whether each pixel in the specific row is going to be saturated at the next integration period. This binary information is saved locally in the 1-bit in-pixel memory, and is transmitted to the external digital storage in the upper part of the sensor, associated with each pixel. Then, if any of the checks determines that the pixel will saturate at the end of the current integration time, the pixel is reset again and is allowed to start integrate light again, but for a shorter period of time. Note that this operation is applied simultaneously to all pixels in the array to guarantee snapshot operation. This operation enables proper scaling of the value being read out and enables the pixel value to be described in a floating-point representation (4). This way, the actual pixel value would be:

$$\text{Value} = \text{Man} \left( \frac{T_{\text{INT}} / X^{\text{EXP}}}{T_{\text{INT}} / X^{\text{EXP}}} \right) = \text{Man} \cdot X^{\text{EXP}}$$

(4)

where Value is the actual pixel value, Man (Mantissa) is the analog or digitized output value that has been read out at the time point $T_{\text{INT}}$, EXP is the exponent value, that is stored in the digital memory block and describes the scaling factor, i.e. which part of the integration time is actually effective. The exponent value is retrieved from a digital memory also at the end of overall integration time $T_{\text{INT}}$.

### B. Threshold Voltage Considerations

The overall idea of the algorithm is to avoid the effect of pixel saturation. As previously mentioned, the algorithm checks a threshold point at first sub-integration period and takes a decision based on the anticipation that during the whole integration period the pixel will not be saturated. Therefore, assuming that $\Delta t_{k} = 0$, meaning that the pixel value was first compared at $T_{\text{INT}} \cdot \left( T_{\text{INT}} / X^{i} \right)$, the intrinsic (theoretical) threshold value $V_{\text{th}, i}$ should be chosen in such a way so that a straight line (dash-dotted line number 1 in Figure 2), that describes discharging of the pixel during $T_{\text{INT}}$, through $V_{\text{reset}}$ (photodiode reset voltage) at $t=0$ and threshold voltage $V_{\text{th}, i}$ at the first sub-integration period will not cross the pixel saturation voltage $V_{\text{sat}}$ before the whole integration time $T_{\text{INT}}$ is due.

The equation of this straight line is given by:

$$V(t) = V_{\text{reset}} - \frac{V_{\text{pixel, DR}}}{T_{\text{INT}}} \cdot t$$

(5)

$V_{\text{pixel, DR}}$ is a maximum pixel voltage swing that is the difference between $V_{\text{reset}}$ and $V_{\text{sat}}$ values. To find the value of the intrinsic threshold voltage $V_{\text{th}, i}$, the $T_{\text{INT}} \cdot \left( T_{\text{INT}} / X^{i} \right)$ is substituted into the line equation, resulting in the following formula:

$$V_{\text{th}, i} = \frac{V_{\text{pixel, DR}}}{X^{i}} + V_{\text{sat}}$$

(6)

In real designs each comparator has its own offset voltage. Therefore, for two different comparators having two different offset voltages the comparison will be performed at different points even if the same threshold voltage $V_{\text{th}, i}$ was set. Figure 2 shows an example of two pixels, discharging by the same illumination level and being processed using two comparators having different offsets. The same $V_{\text{th}, i}$ was applied for both cases. As can be seen, there is an immunity to change in comparator offsets, since in both cases the final results are the same. In the first case (shown by the solid line number 2), the pixel value didn't pass the threshold voltage $V_{\text{th}, i}$ and therefore it was not reset at the first check. In the second case (shown by the dashes line number 3), the pixel value did pass the threshold voltage $V_{\text{th}, i} + V_{\text{offset}}$ and therefore it was reset at the first check. However, the final results (given by equation (4)) remain similar for both cases. Note, in the second case the SNR of the pixel is reduced since the integration time was reduced in this case.

![Figure 1. General architecture of the proposed wide DR global shutter APS.](image1)

![Figure 2. Threshold voltage derivations](image2)
be taken into account when the threshold voltage is calculated. The threshold voltage \( V_{th} \) is now given by:

\[
V_{th} = V_{th,i} + |V_{offset}| \quad (7)
\]

In the present snapshot WDR algorithm implementation there is a certain delay between comparison times of different rows (\( \Delta t_i \neq 0 \) and therefore the difference in time between row \( k \) and row \( i \) is given by (\( \Delta t_i - \Delta t_k \)) - see equation (3)) since the comparison is done in row by row manner, but the final result is not affected. The reason for this immunity to comparison time differences can be explained by the fact that the difference in comparison time is equivalent to the differences in comparator offsets. For example, if pixel values in row \( i \) are compared to \( V_{th} \) at \( T_i \) and pixel values in row \( k \) are compared to \( V_{th} \) at \( T_k \) using the same comparator, this is equivalent to the case when pixels in both rows are compared at the same time \( T \) but using different comparators having different offsets voltages \( V_{offset,i} \) and \( V_{offset,k} \), resulting in different \( V_{th} \) (\( V_{th,i} \) and \( V_{th,k} \)) for each row.

The following explanations are with reference to Figure 3 and assuming \( \Delta t_i >> T_{decision} \). The threshold voltage \( V_{th,n} \) for the pixel array, operated in snapshot mode, is chosen to be higher than \( V_{th} \) in order not to allow saturation of pixel \( A \) in the first row and pixel \( B \) in the last row during one saturation detection check \( \Delta t_i \). \( (\Delta t_i - \Delta t_j) \) is the total time required for the saturation detection process for all rows in an \( N \) by \( M \) array, where \( N \) is number of rows and \( M \) is number of columns (see Figure 3).

By substituting value of \( V_{th} \) from equation (7) into (8)

\[
\frac{V_{pixel, DR} - V_{th,n}}{V_{pixel, DR} - V_{th}} = \frac{T_{INT} - (T_{INT} \frac{X}{X'}) - \Delta t_i}{T_{INT} - (T_{INT} \frac{X}{X'})} \quad (8)
\]

We get the \( V_{th,n} \) value:

\[
V_{th,n} \geq V_{pixel, DR} \left( \frac{-\Delta t_i}{T_{INT} - (T_{INT} \frac{X}{X'})} (1 - V_{th}) - V_{th} \right) \quad (9)
\]

where \( V_{th} \) is given by (7) and \( \Delta t_i \) is defined in (3).

\[
V_{th,n} \geq V_{pixel, DR} \left( \frac{-\Delta t_i}{T_{INT} - (T_{INT} \frac{X}{X'})} (1 - V_{th}) - V_{th} \right) \quad (10)
\]

IV. PIXEL DESCRIPTION AND OPERATION

This sub-section describes the proposed pixel and explains the general principle of its operation. Figure 4 shows the general architecture of a single pixel and its corresponding processing circuitry and a digital memory. Both the processing circuitry and a digital memory are located in the array periphery.

The proposed pixel consists of: (1) Photodiode, (2) Photodiode Reset switch, controlled by \( AND \) gate output, (3) Shutter switch, (4) 1-bit in-pixel digital memory (both static and dynamic memories can be implemented), (5) Analog buffer for analog signal readout, (6) Row Select switch, (7) \( AND \) gate to control locally reset operation of the pixel and (8) \( FD \) Reset switch, used to reset the floating diffusion capacitance \( C_{FD} \). The processing circuits consist of \( AND \), two \( OR \) and \( Latch \) logical elements. In addition, analog Comparator is employed to compare the pixel output to the predefined threshold voltage (\( V_{th,n} \)). Note, both the processing circuit and the pixel, presented in this paper can be designed in different ways, while still implementing the described algorithm. Herein, only one processing circuit and two different pixel examples are presented in detail.

The presented circuit operates as follows: at the beginning of the frame the photodiode capacitance \( C_{FD} \) is reset by applying "Array Reset" = '1' and by loading the high digital value '1' to the in-pixel memory by applying "Global Reset"=’1’. The Shutter switch is "off" during the reset period.

\[
V_{th,n} \geq V_{pixel, DR} \left( \frac{-\Delta t_i}{T_{INT} - (T_{INT} \frac{X}{X'})} (1 - V_{th}) - V_{th} \right) \quad (10)
\]

![Figure 4. Schematic of a single pixel and its corresponding processing circuitry and digital memory.](image)

The reset phase is stopped by applying "Array Reset" = '0' and the photodiode capacitance \( C_{FD} \) starts discharging, according to the energy of incident light. During the photodiode integration period the "Global Reset"=’0’. Before reaching the certain time, when the first row pixels start comparison (\( T_{INT} - (T_{INT} \frac{X}{X'}) - \Delta t_i \)), the \( C_{FD} \) capacitor is pre-charged to \( V_{th,n} \) voltage using the \( FD \) Reset switch.

Once the \( C_{FD} \) precharge is completed, the \( Shutter \) switch is switched "on" and allows charge transfer between the photodiode capacitance \( C_{PD} \) and \( C_{FD} \) floating diffusion capacitance. The voltage on the
photodiode capacitor at the end of this charge transfer is similar to
the voltage that could be achieved by discharging the photodiode
$C_{PD}$ and $C_{FD}$ capacitances connected together from the beginning of
the integration. This is shown in Figure 5. The Shutter switch
remains switched "on" till the end of the integration time $T_{INT}$.

\[
V_{reset} + C_{PD} + C_{FD} 
\]

\[
\text{Shutter turns on}
\]

\[
T_{INT} - (\frac{T_{INT}}{X}) - \Delta t
\]

\[
T_{INT}
\]

\[
V_{sat}
\]

Figure 5: Charge sharing between photodiode capacitance and floating
diffusion capacity

For a pixel in row $k$, at the first time point $T_i = T_{INT} - (\frac{T_{INT}}{X}) - \Delta t_k$ (see equation 2) the voltage on the photodiode capacitance $V_{PD}$ is read out using the analog buffer and is
compared with an appropriate threshold $V_{th\_map}$. The comparator
result is transmitted directly to the in-pixel memory and to the
external digital memory, associated with the pixel ("First bit"="1" is applied).
In case $V_{PD} < V_{th\_map}$, meaning that the pixel will saturate
at the end of the integration time, both mentioned memories are
loaded with '1'. Otherwise, $V_{PD} > V_{th\_map}$, meaning that the pixel
will not saturate at the end of the integration time), '0' is loaded to the
memories. The described process is then sequentially repeated for
each row.

At the $(T_{INT} - (\frac{T_{INT}}{X})$ time point, the "Array Reset" signal is
activated and the photodiodes in all pixels in the array are reset (or
not), according to the data saved in the in-pixel memories. These
simultaneous resets ensure the global shutter operation of the imager.

At the time point $(T_{INT} - (\frac{T_{INT}}{X}) - \Delta t)$, the voltage on the
photodiode $V_{PD}$ is read out and is compared again with an
appropriate threshold $V_{th\_map}$. The binary information concerning
having the reset applied at $(T_{INT} - (\frac{T_{INT}}{X})$ time point, or not, is
retrieved from the corresponding digital memory (input to Latch in
Figure 4) and "AND"ed with the result of the photodiode voltage
comparison with $V_{th\_map}$ ("First bit"="0" is applied). In case that
$V_{PD} < V_{th\_map}$ and the retrieved digital data is '1' (meaning that pixel
was reset at the previous time point), both in-pixel and external
memories are loaded with '1' and the pixel will reset again. In case
$V_{PD} < V_{th\_map}$ but the retrieved digital data is '0' (meaning that the
pixel was not reset at the previous time point), both in-pixel and
external memories are loaded with '0' and the pixel will continue
integration without reset. Finally, if $V_{PD} > V_{th\_map}$, independent of
the retrieved data, both in-pixel and external memories are loaded
with '0' and the pixel will continue integration without reset. At the
$(T_{INT} - (\frac{T_{INT}}{X})$ time point, the "Array Reset" signal is activated
again and the photodiodes in all pixels in the array are reset (or not),
according to the data saved in the in-pixel memories. The same
process is performed for all pixels in the array for all remaining time
points $(T_{INT} - (\frac{T_{INT}}{X}) - \Delta t_t)...(T_{INT} - (\frac{T_{INT}}{X}) - \Delta t_t)$.

At the end of the full integration time $T_{INT}$, the capacitor $C_{PD}$ is
disconnected from the photodiode by turning off the Shutter switch.
Once this charge transfer has been completed, the photodiode is able
to begin a new frame exposure, and the charge on $C_{PD}$ is held there
until it is read out at its assigned time in a row-by-row readout sequence
through the output chain. The value of the readout signal is
associated with the analog value $Man$ (see equation 4). The exponent
value is retrieved from a digital memory also at this time.

In order to improve the performance of the imager, $\Delta_t$ should
be kept as small as possible and reduction in $T_{decision}$ is required. As
previously mentioned, $T_{decision}$ is the time, required to decide whether
each pixel in the specific row is going to be saturated at the next
integration slot and than reset or not. Therefore it can be described as:

\[
T_{decision} = T_{mem\_read} + T_{comp} + T_{mem\_write}
\]

where $T_{mem\_read}$ is the time required to retrieve the digital
information from the memory during decision process (the algorithm
relies on previous stored information), $T_{comp}$ is the time required to
accomplish the digital processing and photodiode voltage comparison
and $T_{mem\_write}$ is the time required to write the digital information
into the memory.

Figure 6 show possible transistor implementations of the proposed
imager pixel. Figure 6(a) shows the implementation where the static
in-pixel memory is used, while Figure 6(b) presents the dynamic
in-pixel memory.

Figure 6: Pixel implementation with a) static in-pixel memory, b) dynamic
in-pixel memory.

III. SIMULATION RESULTS

A test chip having two different 64x64 sensor arrays has been
implemented in a standard TSMC 0.18µm CMOS technology
available through MOSIS. The implemented arrays differ by their
in-pixel 1-bit memory design: while the pixels in the first array employ
in-pixel static memory, the dynamic memory is used in the second
array. Figure 7 shows an example of the pixel layout employing the
static in-pixel memory. Each pixel has a size of 7µm x 7µm and a fill
factor of 20% for the static memory case and of 25% for the dynamic
memory case.

Figure 7: Pixel layout, employing in-pixel 1-bit static memory.
Figure 8 presents an example of a single pixel simulation. The simulation has been carried for $T_{\text{INT}} = 30\, \text{msec}$ for two different illumination levels.

The figure shows the voltages on the photodiode $V_{\text{PD}}$, on the $C_{\text{FD}}$ capacitance $V_{\text{C}_d}$, and the value stored in the in-pixel 1 bit memory ("in_pixel_mem") for two sequential frames. Two bit DR expansion was applied, i.e. comparisons were performed at $T_0 = T_{\text{INT}} - \left( T_{\text{INT}} / X \right) - \Delta t_1$ and $T_1 = T_{\text{INT}} - \left( T_{\text{INT}} / X \right) - \Delta t_2$ with $X=2$ during the first frame and at $T_3 = T_{\text{INT}} - \left( T_{\text{INT}} / X \right) - \Delta t_3$ and $T_4 = T_{\text{INT}} - \left( T_{\text{INT}} / X^2 \right) - \Delta t_4$ during the second frame. $T_3$ indicates the end of the first frame and the start of the second frame. In the presented simulation the illumination level has been decreased at the end of the first frame and the start of the second frame. It can be seen, that for the first frame, $V_{\text{PD}}$ passed the threshold $V_{\text{th, snap}}$, during the first comparison ($T_0$ in Figure 8), meaning that the pixel will saturate at the end of the integration time and therefore the pixel was reset and ‘1’ was written into the in-pixel digital memory. For other comparisons (at $T_1$, $T_3$ and $T_4$), $V_{\text{PD}}$ didn’t pass the threshold $V_{\text{th}}$, meaning that the pixel will not saturate at the end of the integration time and therefore the pixel was not reset and ‘0’ was written into the in-pixel digital memory.

Figure 9 zooms in to the first comparison during the first frame ($T_0$ in Figure 8). $T_0.1$ time point indicates the time when the $C_{\text{FD}}$ capacitor is reset using $FD_{\text{Reset switch}}$ (see Figure 4), $T_0.2$ time point indicates the operation of the $Shutter_{\text{switch}}$ when the charge transfer between the photodiode $C_{\text{PD}}$ and $C_{\text{FD}}$ capacitances occurs.

Finally, at $T_0.2$ time both the photodiode and $C_{\text{FD}}$ capacitor are reset, according to the comparison result. A variety of additional simulations were carried out to ensure proper system operation.

IV. CONCLUSIONS AND FURTHER RESEARCH

A novel concept for global shutter CMOS image sensors with Wide Dynamic Range (WDR) implementation was presented. The proposed imager provides wide DR by applying adaptive exposure time to each pixel, according to the local illumination intensity level. Different pixel configurations were designed and simulated. A test chip, having 64x64 arrays has been implemented in a standard TSMC 0.18µm CMOS technology. System architecture and operation were discussed and simulation results were presented.

Further research includes fabrication of the proposed sensor and testing.

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REFERENCES