Advanced output chains for CMOS image sensors based on an active column sensor approach—a detailed comparison

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Abstract

A detailed comparison between four types of pixels, based on a CMOS active column sensor (ACS) output chain technique is presented. A test chip of $64 \times 64$ pixels consisting of four $16 \times 64$ arrays, each with a different output chain, has been implemented in 0.35 μm CMOS technology available through MOSIS and operated via a 3.3 V supply. The chip includes four different amplifier/pixel combinations: (a) an n-channel based voltage amplifier with an n-channel reset transistor, (b) an n-channel based voltage amplifier with a p-channel reset transistor, (c) a p-channel based voltage amplifier with an n-channel reset transistor, (d) a p-channel based current mirror with an n-channel reset transistor. Pixel and output chain architectures are discussed, their operation is explained, simulations results are presented and measurements from a test chip are reported.

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1. Introduction

Active pixel sensors (APS) are meant to achieve the idea of a “camera on a chip” [1]. Unfortunately, there are issues with the fundamental APS approach that limit performance and functionality. The fundamental concept of the APS is to place an amplifier inside each pixel. This provides a good signal level coming out of the pixel with lowered supply voltages, comparable to the signal levels emerging from a CCD that utilizes higher supply voltages.

In the making of a CMOS active pixel sensor several factors affect the quality of the sensor: the sensitivity of the pixel, the noise generated during the operation, and the accuracy of the electrons to voltage conversion. The term sensitivity describes the ability of the APS to convert photons striking the area of the pixel to a voltage potential, thus defining the sensitivity of the pixel as the potential generated per photon and measured in V/Lux. Sensitivity could be improved by optimizing the pixels design, i.e. tuning the active area shape, fill factor, and other parameters. Noise, both temporal and spatial is generated during pixel operation (reset, integration, and readout phases), and by the readout circuitry. A rigorous effort has been done to analyze and elevate this inherent problem [2–5]. Charge to voltage conversion is performed by the active part of the pixel—the amplifier; this unit must reflect the changes in the accumulated charge as accurately as possible, and produce a true linear output signal. The in-pixel amplification is part of the so-called output chain, consisting of many stages processing the photo-signal. This work focuses on the optimization of the in-pixel amplifier and output swing enhancement via modification of the reset transistor.

Many works on signal enhancement and output chain improvement have been published in the literature [6–9]. Most works focused on the common column stages improvement, such as delta difference sampling (DDS) and correlated double sampling (CDS) [8,9], without changing the in-pixel amplifier architecture. Usually, a standard 3-transistor APS utilizes a source follower transistor for amplification causing gain and offset mismatches. The active column sensor (ACS) approach, first presented in [6], solved this problem using a true in-pixel unity gain amplifier (UGA), without increasing the number of transistors utilized by the pixel and thus maintaining a high fill factor. An n-channel reset transistor and one stage n-channel differential amplifier were used in that work.
Our work enhances the ACS technique by means of current/voltage amplification, reset voltage enhancement and UGA improvement. A test chip of $64 \times 64$ pixels consisting of four $16 \times 64$ arrays having different output chains has been implemented in 0.35 $\mu$m CMOS technology to compare different ACS-UGA techniques.

The remainder of the paper is organized as follows: Section 2 explains the concept of the standard 3-transistor photodiode CMOS APS and describes the existing ACS approach and shows four different ACS techniques implemented in our work. The measurements from a test chip are presented in Section 3. Section 4 concludes the paper.

2. Active column sensor approach

2.1. CMOS photodiode APS

A standard photodiode APS consists of a floating reverse biased p–n junction, with three transistors and four conductors per pixel, a sense node connected to the gate of a source follower (SF) transistor M2, a reset transistor M1 and a row select (RS) transistor M3, as shown in Fig. 1.

Examining the APS performance shows a design tradeoff. Noise and full-well trade, as we try to maximize the accumulated charge through well size enhancement the noise performance degrades. Moderately high quantum efficiency, and easy to implement in advanced sub-micron technology completes the three transistors APS brief description.

The SF acts as a charge amplifier. Ideally, the SF should be avoided and replaced with a real UGA. Unfortunately, it is impossible to squeeze a full UGA into each pixel, while retaining a good fill factor and acceptable pixel area [6]. APS devices typically use a small geometry source follower amplifier inside the pixel in order to minimize the area occupied by the amplifier. The SF amplifier characteristics vary from pixel to pixel due to inherent process deviations in the $V_T$ voltage, mobility, oxide thickness, and gate length. Two main factors that affect the homogenous performance of the APS exist:

(1) Gain variations due to the transconductance variation of the SF (transistor M2 in Fig. 1) cause varying signal levels from different pixels, even for homogenous levels of illumination. The pixel-to-pixel gain variations lead to a visible fixed pattern noise (FPN).

(2) Non-uniformities due to variations across the SF load transistor, usually located at the bottom of each column. This causes column-to-column FPN due to resistance variations of the channel.

An additional parameter affecting signal amplification is the voltage gain of a SF that ideally equals unity. However, the real transfer function is bulk effect (or “back-gate effect”) dependent and in normal operation is equal to:

$$\frac{g_m}{g_m + g_{mb}} \approx 0.86$$

where $g_m$ is the transconductance and $g_{mb}$ the back-gate effect coefficient. Thus, the voltage at the gate of the SF is further attenuated.

Another major performance reduction in APS operation is the reset voltage amplitude. Since the capacity of the potential well is limited by the maximum applied reset voltage, it is highly desirable to maximize the reset voltage. When looking at the signal path from the gate of M1 (Fig. 1) to the output node—source of M2, a drop of at least $2V_T$ could be observed. Unfortunately, the body effect affects these $V_T$s as well. In an APS pixel, fabricated in a standard 0.35 $\mu$m CMOS technology and operated by a 3.3 V supply, the source-bulk potential can build up to 2.3 V and the effective $V_T$s can increase up to 1.1 V instead of $V_Ts \sim 0.5$ V. As a result, the effective reset voltage is $\sim 1.6$ V instead of 3.3 V at 3.3 V supply voltage. This further reduces the dynamic range of the APS.

2.2. Active column sensor techniques and analysis

The gain variation existing in a conventional APS can be eliminated by utilizing a full UGA per pixel. However, adding six or more in-pixel transistors will severely affect the area of the APS. The ACS approach was first introduced in [6] to allow an in-pixel UGA implementation, while maintaining a high fill factor. Fig. 2 shows the basic ACS pixels, as presented in [6]. The ACS method divides the UGA structure into two sub-structures: the first situated inside the pixel (transistors M2k and M3k in Fig. 2), while the second part (transistors M4–M8 in Fig. 2) resides at the bottom of the column and is common to all pixels in that column. This way the fill factor and pixel properties are not affected, while a true UGA is achieved. The UGA itself is formed through a differential pair (transistors M3k and M6) with active load transistors M7 and M8. Note, that M2k is the standard row select switch, while M5 is added for symmetry reason (always biased at $V_{dd}$).

It can be seen that only three transistors are needed per pixel: the reset transistor, the input signal differential transistor and the selection transistor. This structure enables flexibility as found in the standard CMOS sensor, i. e. random access, self-clocking, low power, etc. Note, that in order to eliminate the amplifier offsets, a CDS circuit is required for every column.
The existing ACS approach utilizes a one stage simple UGA. This paper presents four different approaches utilizing a modified reset transistor and an improved UGA via the following combinations: (a) an n-channel based voltage amplifier with an n-channel reset transistor, (b) an n-channel based voltage amplifier with a p-channel reset transistor, (c) a p-channel based voltage amplifier with an n-channel reset transistor and (d) a p-channel based current mirror with an n-channel reset transistor.

The principle scheme of the ACS pixel structures used in our work is shown in Fig. 3. Description and analysis of the UGA amplifiers are presented in the following subsections.

2.2.1 ACS using NMOS reset and NMOS differential pair

An n-channel reset with n-channel differential pair ACS pixel used in our work can be seen in Fig. 3a. Only three transistors per pixel are needed—no modification to the basic structure. Since the gain can now be set to unity the voltage transfer function could be improved by 15%. Using n-channel transistors as a differential pair has a great advantage due to the high fill factor and the fact that no change to the pixel layout is needed. In some cases the fill factor can be up to 70% depending on the pixel and transistors size.

The UGA that had been used in this design (Fig. 4b) is based on the standard and well known two-stage operational amplifier architecture, although designs with improved characteristics can be implemented with the ACS architecture. The design of the amplifier is very straightforward, but in our case there is a constraint on the area occupied by the differential pair in order to retain a high fill factor and a small pixel pitch.

The amplifier actually has three stages: two gain stages and one output stage. The first gain stage is a differential-input to single ended output stage; the second gain is a common-source gain stage with an active load. Capacitor Cc ensures the stability of the opamp in a UGA configuration. Note that due to the column parallel implementation of the ACS system, column half differential-pair pixels are all connected to the same node causing capacitive loading of the UGA. The stability of the UGA is decreased due to capacitive loading of the column, and calls for higher capacitive compensation within the opamp. A detailed parameter analysis is presented for a p-channel differential pair in the next section.

Although n-channel usage has an advantage due to its compact area consumption, it also has a disadvantage because of its low ability to convey lower voltage levels that represent high illumination.

When using an n-channel reset transistor there is a $V_T$ drop over the reset transistor and the pixel undergoes soft
reset. This scheme is shown in Fig. 3a. Soft reset has a noise advantage over hard reset (presented in the next subsection) [5], but causes a higher lag.

2.2.2. ACS using PMOS reset NMOS differential pair

A p-channel reset with n-channel differential pair ACS pixel is shown in Fig. 3c. While only three transistors per pixel are used, the modified pixel now consists of a p-channel reset transistor. Due to well spacing requirements the fill factor of the pixel is severely decreased. For example, a 0.35 μm process pixel with an area of 7 μm × 7 μm with an n-channel reset transistor has a 39% fill factor, while the same pixel with a p-channel reset transistor will have only 16% fill factor—a 60% drop. On the other hand, p-channel reset usage allows hard reset to the pixel, thus eliminating the $V_T$ drop and lowering the image lag. The performance of the UGA stays the same as in the previous description.

2.2.3. ACS using a PMOS differential pair

The concept of this technique is the same as the one described in Section 2.1 with only one main difference—the UGA now has a p-channel differential pair (Fig. 4a) while retaining a soft reset operation (n-channel reset transistor). Using p-channel transistors as a differential pair poses a great advantage due to the ability to convey low voltage signals emitted from the photodiode occurring at high illumination.

The following is an analysis of the p-channel differential amplifier. Note that with minor modification this can serve as the n-channel amplifier’s analysis.

The gain of the first stage is given by:

$$A_{V1} = \frac{g_{m1}(V_{ds1})}{r_{ds1}}$$  (1)

where $g_{m1}$ is the transconductance of the in-pixel half differential pair and is given by:

$$g_{m1} = \frac{1}{2}\mu pC_{ox}\left(\frac{W}{L}\right)\frac{I_{bias}}{2}$$  (2)

where $I_{bias}$ is formed by transistors M10–M13 as shown in Fig. 4.

As can be seen from Eqs. (1) and (2), the minimal $W/L$ used at the in-pixel input transistors causes a gain decrease in the first stage. The second gain stage is added to compensate...
for the low gain of the first stage. A common-source gain stage with a p-channel active load is used as the second stage. Following is the gain of this stage:

\[ AV_2 = g_{m7} (r_{ds6} || r_{ds7}) \]  

The third stage is a common-drain buffer stage (source follower). The source follower gain is given by:

\[ AV_3 = \frac{g_{m8} G_L + g_{m8}}{g_{m8} + g_{ds8} + g_{ds9}} \]  

where \( G_L \) is the load conductance being driven by the buffer stage and \( g_{mb8} \) the body effect conductance and is given by:

\[ g_{mb8} = \frac{g_{m2} \gamma}{\sqrt{V_{SB} + 2\phi_f}} \]  

where \( V_{SB} \) is the source to substrate voltage and \( \gamma \) the body effect constant.

Open loop frequency response is calculated on the assumption that capacitance except the compensation capacitor are ignored. The second stage introduces capacitive load on the first stage due to the compensation capacitor. If we assume that the gain of the output stage is approximately 1, then the overall gain simplifies to:

\[ AV(s) = \frac{g_{m1}}{3C_c} \]  

Defining the slew rate SR as:

\[ SR = \frac{dV_{out}}{dt} \bigg|_{\text{max}} = \frac{I_{c\text{max}}}{C_c} = \frac{I_{D10}}{C_c} \]  

Since \( I_{D10} = 2I_{D10\text{max}} \) we can write:

\[ SR = \frac{2I_{D1}}{C_c} = \frac{2I_{D10\text{max}}}{g_{m1}} \]  

The final relationship for the slew rate is given by:

\[ SR = \frac{2I_{D1}}{\sqrt{2} \mu_p C_{ox} (W/L)(I_{D10\text{max}})} \]  

It can be seen that obtaining a high slew rate and unity gain frequency are two of the major reasons for choosing p-channel input transistors rather than n-channel input transistors.

### 2.2.4. ACS using a current mirror

An ACS using a current mirror output chain has the same advantages as an n-channel UGA with a soft reset mechanism. The basic structure of the pixel stays the same and

<table>
<thead>
<tr>
<th>Table 1</th>
<th>UGA measured characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>p-Channel UGA</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>23.2 V/μs</td>
</tr>
<tr>
<td>Maximum settling time to 1%</td>
<td>0.273 μs</td>
</tr>
<tr>
<td>Output voltage swing</td>
<td>0.2-3.4 V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>24.75 mW</td>
</tr>
</tbody>
</table>
there is no need to re-design the pixel. There are fewer tran-
sistors than in a UGA configuration and the slew rate/power
dissipation can be directly traded-off since there is only one
current node. Current mirrors are less sensitive to mismatch
and occupy less area. With this configuration only one \( V_T \)
is lost (the potential drop over the reset transistor) and is
returned by the mirror transistor. One major draw-back is a
column \( I \times R \) drop since current is being conveyed to the
sample capacitor. A current mirror pixel is shown in Fig. 3d
and a current output chain is shown in Fig. 4c.

### 3. Performance and test chip measurements

The \( 64 \times 64 \) APS test chip was fabricated in a \( 0.35 \mu \text{m}, \)
n-well, four metal, CMOS, TSMC technology process sup-

![](image)

Fig. 6. (a) Input scene to the ACS test chip, (b) the part of Ben-Gurion University logo, as captured by the fragmented ACS array.
ported by MOSIS. The supply voltage is 3.3 V. The photogra-
photograph of the fabricated test chip and the zoomed UGA
area is shown in Fig. 5. As can be seen in Fig. 5b every 16 ×
64 pixels sub-array contained a different pixel/output
chain configuration.

The test chip was designed in a way that enables modular
testing of every functional block of the chip separately, as
well as measurements of the whole chip.

Table 1 is a summary of the p-channel and n-channel
UGAs characteristics. Experimental results from the differ-
ext of the two configurations is different. The soft reset (column
3) p-channel UGA configuration can accommodate high il-
1umination level. On the other hand, the hard reset (column
4) n-channel UGA can accommodate for low light level il-
1umination while saturating in response to high light levels.
The current mirror approach can accommodate either high
or low illumination level, but as can be observed from Table 2,
it has the higher non-linearity relatively to other implemented
techniques.

4. Conclusions

A comprehensive comparison between four types of pix-
eels, based on a CMOS active column sensor output chain
technique has been presented. A test chip of 64 × 64 pix-
eels consisting of four 16 × 64 arrays each with a different
output chain has been implemented in 0.35 μm CMOS tech-
nology available through MOSIS. The properties of these
pixels had been compared to the standard 3-T APS with re-
spect to the potential drop in the reset and signal levels, and
fill factor. A theoretical analysis of the p-channel differen-
tial UGA that can easily be applied to the n-channel UGA
has been provided.

The experimental results show that an ACS approach
using n-channel input UGA has some advantages over the
p-channel input UGA: a higher fill factor and low illumination level computability. The ACS technique
using a p-channel input UGA has some advantages over
the n-channel input UGA: a higher slew rate, a higher
unity gain frequency and high illumination level com-
putability. The current mirror approach can accommo-
date either high or low light levels, but has a higher
non-linearity relative to the other implemented tech-
niques.

Both p-channel and n-channel reset transistors have been
tested. The p-channel reset transistor provides hard reset and
thus an increased output swing when used with an n-channel
UGA, but cannot be used with the p-channel UGA, retain-
ing a reasonable fill factor. Using an n-well based photo-
diode can maximize the pixel fill factor with a p-channel
UGA.

In conclusion, using the ACS technique is highly desir-
able since there is almost no area penalty. It is most desir-
able to use the PMOS based UGA implementation with the
NMOS reset transistor due to its high linearity, high output
swing, medium power consumption and fill factor. Most of
all this implementation is suitable low and high illumination
scenes.

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Shai Diller was born in Tel-Aviv, Israel, in 1972. He received the BSc degree from Ben-Gurion University, Beer-Sheva, Israel, in 2001 in electrical engineering. He is currently working toward the MSc degree in electro-optical engineering at Ben-Gurion University.

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Alexander Fish was born in Kharkov, Ukraine, in 1976. He received the BSc degree in electrical engineering from Technion, Israel Institute of Technology, Haifa, Israel, in 1999, and an MSc degree in electrical engineering from Ben-Gurion University, Beer-Sheva, Israel, in 2002. He is currently working on his PhD degree in electro-optics engineering at Ben-Gurion University.

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Orly Yadid-Pecht received her BSc from the Electrical Engineering Department at the Technion, Israel, Institute of Technology in 1983. She completed her MSc in 1990 and her DSc in 1995, respectively, also at the Technion. She was a research associate of the National Research Council (USA) from 1995 to 1997 in the area of Advanced Image Sensors at the Jet Propulsion Laboratory (JPL)/California Institute of Technology (Caltech). In 1997 she joined the Ben-Gurion University in Israel, as a faculty member in the Electrical and Electro-Optical Engineering Departments. There she founded the VLSI Systems Center, specializing in CMOS image sensors.

Her areas of interest are integrated CMOS image sensors, smart sensors, image processing, neural nets and pattern recognition algorithms implementation. She has published dozens of papers and patents and has led over 10 research projects supported by government and industry. She was an associate editor for the IEEE Trans. on VLSI journal and is currently the deputy editor in chief for the IEEE Trans. on CAS-I journal, the chair of the IEEE CAS sensors technical committee and a member of the neural networks and analog technical committees, a member of the technical committee for the IEEE bi-annual workshop on CCDs and advanced image sensors, and a member of the SPIE solid state sensor arrays program committee. Currently, she is also the general chair of the IEEE International Conference on Electronic Circuits and Systems (ICECS) that will be held in Israel in 2004.