A Snapshot CMOS Image Sensor With Extended Dynamic Range

Alexander Belenky, Alexander Fish, Member, IEEE, Arthur Spivak, and Orly Yadid-Pecht, Fellow, IEEE

Abstract—In this paper, a proof of concept for a snapshot CMOS image sensor with extended dynamic range is presented. A prototype of 32 × 32 pixels has been fabricated using the 1-poly 4-metal CMOS 0.35 μm process available through MOSIS and was successfully tested. The measurements from the test chip showed that the fabricated imager allows wide dynamic range (WDR) operation in a snapshot readout mode. This DR extension has become possible due to a unique in-pixel architecture allowing automatic adaptation of each pixel in the array to its illumination level. To reduce the pixel power dissipation various low-power design techniques have been utilized in the pixel design. A single pixel occupies $18 \times 18 (\mu m)^2$ and dissipates 23 nW with 8 bit DR expansion at room light level, and 29 nW at high illumination level, equivalent to clear sky at video rate. The power dissipation of the whole sensor (including the supporting circuitry) is 450 μW at video rate. Sensor design is described, design considerations are shown and measurements from the test chip are presented.

Index Terms—CMOS imagers, high dynamic range, image sensor, integration time, low-power, very large scale integration (VLSI).

I. INTRODUCTION

AST development of low-power miniature CMOS image sensors triggers their penetration to various fields of our daily life. CMOS imagers offer significant advantages in terms of low-power, low-voltage, flexibility, cost, and miniaturization. These features make them very suitable for a variety of applications where both low-power and wide intrasence dynamic range (WDR) are the main demands. While power reduction is usually achieved by technology scaling and aggressive supply voltage reduction [1], it however affects the output swing of the sensor and thus decreases its dynamic range (DR) [1]–[3]. The narrow DR of image sensors entails saturation of a pixel with high sensitivity, in case of high illumination levels, and part of the information can be lost. DR insufficiency of conventional video cameras is a serious problem in realizing a robust vision system for taking images consisting of wide illumination conditions in the same scene.

Different solutions for extending the DR in CMOS image sensors have been presented in recent years [5]–[30]. A comprehen-
Another variation of the multiple exposures algorithm was presented in [24] and [25], where the shorter integration time overlapped the longer one. During the integration, the array was reset to some intermediate well potential. Pixels that did not pass the mid-point barrier continued to integrate without intermediate information loss. The information loss caused by the mid-point reset was compensated by autoscaling the charge accumulated during the shorter exposure time. Consequently, the signal-to-noise ratio (SNR) in low light intensity was improved in comparison to regular multiple exposures algorithm; (g) Sensors with local control, where different areas within the sensor can have different exposure times [26]; and (h) Sensors with autonomous control over the integration time, in which the integration time is adjusted by each pixel [27]–[30]. The imager described in this paper is based on this method. This method can be regarded as a multi-reset algorithm and utilizes the conditional reset scheme, which is implemented at the pixel level. The pixel structure remains simple and the final signal processing is very straightforward, i.e., the data is being integrated on the pixel capacitance; followed by readout of the signal and reset levels for subtraction and final A-D conversion. Thus, there is no need to choose between optional signals received from multiple A-D conversions that are unavoidable in the multimode and the multiple exposure sensors. Another advantage of the sensors proposed in [27]–[30] is that the threshold value to which the pixel is being compared to is time invariant, thus there is no need to generate highly precise global time varying voltage references.

Conventional CMOS imagers operate in a rolling shutter mode [3] which leads to image deformation in times when there is relative motion between the imager and the scene. The imager, operating in the global shutter (snapshot) regime, utilizing a memory element inside each pixel solves this problem and provides capabilities similar to a mechanical shutter. This allows simultaneous integration of the entire pixel array, and then preventing exposure while the image data is read out.

Recently, we have proposed a new WDR CMOS image sensor architecture that can deal with all of the above mentioned challenges of CMOS image sensors and presented its simulation results [30]. This proposed imager was expected to provide wide DR by applying adaptive exposure time to each pixel, according to the local illumination intensity level. Driven by low-power dissipation requirements, the proposed pixel was designed to operate with dual low-voltage supplies (1.2 and 1.8 V) and utilized an advanced low-power sensor design methodology. This methodology included implementation of a special low-power and area efficient components, such as comparator and multiplexer, as well as various general techniques for power reduction.

The goal of this paper is to provide a proof of concept for the previously designed imager. Since the imager employs nonstandard circuits and utilizes complicated pixels, each consisting of 18 transistors, this proof of concept stage is essential for further snapshot WDR sensor development. This paper presents measurements from a test chip and shows that the fabricated imager is fully operational and allows extension of dynamic range, as expected. In addition, design considerations, such as threshold voltage considerations, low-power considerations, and noise analysis are presented.
be calculated at the end of the integration period by multiplying the final readout level by a scaling factor which is based on the length of time since the last reset. This length of time may be determined from knowledge of how many times the given pixel was reset over the entire integration period. Therefore, the light intensity of the pixel is calculated as

\[ \text{Value} = \text{Man} \cdot X^{\text{EXP}} \]  

(1)

where Value relates to the incident light intensity, Man is the analog or digitized output value that has been read out at the end of the integration period, \(X\) is a chosen constant (\(X > 1\)), for example 2, that relates to the division of the integration time into progressively shorter intervals and \(\text{EXP}\) represents how many times the given pixel was reset over the entire integration period.

The presented circuit operates as follows: at the beginning of the frame the pixel is reset by applying “Global Reset” \(= \text{‘0’}\) and “Cond Reset” \(= \text{‘0’}\). This way the internal line “Reset” is equal to \(\text{‘1 h’} (1.8 \text{ V})\) independently on the internal line “Comp out” value, charging the photodiode (\(C_{\text{pd}}\)) and internal line \(\text{“Comp in”} (C_{\text{comp}}) \) to \(V_{\text{reset}} = V_{\text{DDh}} - V_{\text{thN}} \sim V_{\text{DD}}\),

where \(V_{\text{DDh}} = 1.8 \text{ V (‘1 h’)}\), \(V_{\text{DD}} = 1.2 \text{ V (‘0’)}\) and \(V_{\text{thN}}\) is the threshold voltage of an NMOS. At the same time, the internal line “Comp out” is precharged to “‘1 h’” by negative pulse of “Comp out pre-charge” \(= \text{‘0’}\). The reset phase is stopped by applying “Global Reset” \(= \text{‘1’}\) and “Cond Reset” \(= \text{‘1’}\) and photodiode starts discharging, according to the energy of incident light. At this stage, the total capacitance connected to the photodiode is given by \(C_{\text{pd}}' = C_{\text{pd}} + C_{\text{comp}}\). At the end of the first interval the output of the photodiode (voltage on \(C_{\text{pd}}'\)) is compared with an appropriate threshold, associated with the switching threshold voltage of the comparator, implemented by a conventional inverter. This comparison is performed by enabling the inverter operation (“Sleep” \(= \text{‘1 h’}\) and “not(Sleep)” \(= \text{‘0’}\)).

If “\(C_{\text{pd}}'\) < threshold”, meaning that the pixel will saturate at the end of the integration time, then “\(\text{Comp out}’\) = \(\text{‘1 h’}\) (determined by the inverter). At the same time, “Cond Reset” falls to “‘0’” by applying short negative pulse, causing the \(M_9\) and \(M_{10}\) to operate as a standard inverter and enabling operation of the inverter, consisting of \(M_{11}, M_{12}\) and \(M_{33}\). As a result, (for \(\text{“Comp out”} = \text{‘1 h’}\)) the photodiode is reset again. The binary information concerning having the reset applied or not is saved locally in storage capacitor \(C_{\text{st}}\) by “Read digital” \(= \text{‘0’}\) at the time when \(\text{“Cond Reset”} = \text{‘0’}\) and is transmitted during the next interval to the external digital storage in the upper part of the sensor array, associated with the certain pixel, to enable proper scaling of the value read. The readout of this digital signal is performed through the regular output chain, used for analog signal readout, by allowing “Row Select” \(= \text{‘1’}\).

If “\(C_{\text{pd}}'\) > threshold”, i.e., meaning that the pixel will not saturate at the end of the integration time, then “\(\text{Comp out}’\) = \(\text{‘0’}\) (determined by the inverter). In this case, the photodiode is not reset (“\(\text{Cond Reset”} = \text{‘0’}\), “\(\text{Comp out}’\) = \(\text{‘0’}\) \(\Rightarrow “\text{Reset”} = \text{‘0’}\) and transistor \(M_6\) is turned off, separating \(C_{\text{pd}}'\) and \(C_{\text{comp}}\). Once the comparison is stopped by returning the inverter to the “sleep” mode and applying “Global Reset” \(= \text{‘1’}\) and “Cond Reset” \(= \text{‘1’}\), the photodiode continues discharging, according to the energy of incident light. This time, the total capacitance connected to the photodiode is given only by \(C_{\text{pd}}\). At the end of subsequent intervals (when comparisons are performed again), \(C_{\text{pd}}\) is already disconnected from the \(C_{\text{comp}}\), causing the voltage saved on \(C_{\text{comp}}(> \text{threshold})\) to be compared to the threshold voltage, produced by the inverter. Thus, no resets are applied until the full integration time is finished.

At the end of the full integration time \(T_{\text{INT}}\), the capacitor \(C_{\text{pd}}'\) is connected to the capacitor \(C_{\text{comp}}\) by applying “\(\text{Comp out pre-charge”} = \text{‘0’}\) and the final photodiode voltage on the capacitor \(C_{\text{pd}}' = C_{\text{pd}} + C_{\text{comp}}\) is determined by the charge transfer between \(C_{\text{pd}}'\) and \(C_{\text{comp}}\). This way the final voltage is independent of whether \(M_6\) transistor was closed or open during the last interval. Note, in case, when “\(\text{Comp out”} = \text{‘1 h’}\) (reset was performed at the last comparison), the capacitor \(C_{\text{pd}}\) was already connected to the capacitor \(C_{\text{comp}}\).

The next stage is transfer of the charge accumulated in the photodiode capacitor \(C_{\text{pd}}\) to a storage capacitor \(C_s\), by applying “Shutter” \(= \text{‘1 h’}\). Before this charge transfer, the storage capacitor \(C_s\) is reset to \(V_{\text{DDh}}\) by applying “Storage Reset” \(= \text{‘0’}\). Once this charge transfer has been completed, the photodiode is able to begin a new frame exposure, and the charge, newly transferred to the in-pixel memory, is held there until it is read out at its assigned time in a row-by-row readout sequence through the output chain.
III. DESIGN CONSIDERATIONS

A. Threshold Voltage Considerations

The overall idea of the algorithm is to avoid the effect of pixel saturation. As previously mentioned, the algorithm compares the readout level of each pixel to a respective threshold voltage at the end of each interval and takes a decision based on the anticipation if during the whole integration period the pixel will be saturated or not. Therefore, assuming that the pixel value was first compared at $T_{\text{INT}}$ ($T_{\text{INT}}/X_1$), the intrinsic (theoretical) threshold value $V_{\text{th},i}$ should be chosen in such a way, so that a straight line (dash-dotted line number 1 in Fig. 3) that describes discharging of the pixel during $T_{\text{INT}}$, through $V_{\text{reset}}$ (photodiode reset voltage) at $t = 0$ and the threshold voltage $V_{\text{th},i}$ at the first subintegration period, will not cross the pixel saturation voltage $V_{\text{sat}}$ before the whole integration time $T_{\text{INT}}$ is due.

The equation of this straight line is given by

$$V(t) = V_{\text{reset}} - \frac{V_{\text{pixelLDR}}}{T_{\text{INT}}} t$$

where $V_{\text{pixelLDR}}$ is a maximum pixel voltage swing equal the difference between $V_{\text{reset}}$ and $V_{\text{sat}}$ values. To find the value of the intrinsic threshold voltage $V_{\text{th},i}$, the $T_{\text{INT}} - (T_{\text{INT}}/X_1)$ is substituted into the line equation, resulting in the following formula:

$$V_{\text{th},i} \geq \frac{V_{\text{pixelLDR}}}{X_1} + V_{\text{sat}}.$$  

(3)

In real designs, each comparator has its own offset voltage. Therefore, for two different comparators having two different offset voltages the comparison will be performed at different points even if the same threshold voltage $V_{\text{th},i}$ was set. Fig. 3 shows an example of two pixels, discharging by the same illumination level and being processed using two comparators having different offset values. The same $V_{\text{th},i}$ was applied for both cases. As can be seen, there is an immunity to change in comparator offsets, since in both cases the final results are the same. In the first case (shown by the solid line number 2), the pixel value did not pass the threshold voltage $V_{\text{th},i}$ and, therefore, it was not reset at the first comparison. In the second case (shown by the dashes line number 3), the pixel value did pass the threshold voltage $V_{\text{th},i} + |V_{\text{offset}}|$ and, therefore, it was reset at the first comparison. However, the final results [given by (1)] remain similar for both cases. Note, in the second case, the SNR of the pixel is reduced since the integration time was reduced in this case. A more detailed description on influence of integration time on the sensor SNR can be found in [21]–[23].

Although the sensor provides immunity to the comparator offsets, it is very important to choose the threshold $V_{\text{th}}$ that ensures that all pixels in the array will not saturate at the end of the whole integration period. This threshold voltage $V_{\text{th}}$ is given by

$$V_{\text{th}} = V_{\text{th},i} + |V_{\text{offset}}|.$$  

(4)

where $|V_{\text{offset}}|$ is the absolute value of the maximum comparator offset in the array.

B. Noise Considerations

Noise contribution in the fabricated imager can be classified according to the following noise generation sources: thermal (“reset”) noise induced by reset operation, fixed pattern noise (FPN), caused by process variations and quantum shot noise due to fluctuations in the photo and dark currents. The overall contribution of the “reset” noise in the imager is given by

$$V_{\text{thermal, tot}}^2 = kT \left( \frac{1}{C_{\text{pdj}}} + \frac{1}{C_{\text{comp}}} + \frac{2}{C_s} \right).$$  

(5)

The noise variance resulted in reset operation contributed by the $C_s$ capacitance is doubled since the readout procedure does not utilize true CDS. Assuming that the sensor operates at room temperature, the calculated noise voltage deviation is 1.46 mV.

At the end of integration period, $T_{\text{INT}}$, the final voltage on the $C_s$ capacitance is given by

$$V_{\text{output}} = V_{\text{initial}} - \frac{(i_{\text{ph}} + i_{\text{dc}}) t_{\text{eff}}}{C_{\text{pdj}} + C_{\text{comp}} + C_s}.$$  

(6)

where $t_{\text{eff}}$ is the effective integration time, representing the period from the last reset to $T_{\text{INT}}$ and $V_{\text{initial}}$ is the nominal pixel reset voltage on the $C_s$ sensing node. $V_{\text{initial}}$ is defined by the
In order to calculate the final output voltage \( M_{\text{sat}} \) from (1) that represents the incident light intensity fallen on the pixel, two samples are performed at the end of the integration period. During the first sample, the \( V_{\text{out, pix}} \) is readout, while during the second one the \( V_{\text{init,1}} \) value is sampled. The readout value of the first sample is given by

\[
V_{\text{out,1}} = V_{\text{out, pix}} - V_{\text{bias}} - \sqrt{\frac{I_{\text{bias}}}{K_{\text{in}}}}.
\]

where \( V_{\text{bias}} \) is the SF transistor \( M_{\text{th}} \) threshold voltage, \( I_{\text{bias}} \) is the bias current in the SF and \( K_{\text{in}} \) is the transconductance parameter of the same transistor. The value of the second sample is given by

\[
V_{\text{out,2}} = V_{\text{init,2}} - V_{\text{bias}} - \sqrt{\frac{I_{\text{bias}}}{K_{\text{in}}}}.
\]

C. Low-Power Design Considerations

A number of approaches for power reduction in CMOS image sensors were presented in the literature \[1\], \[31\]. According to these approaches, the power can be reduced at different design levels – technology, device, circuit, logic, architecture, algorithm, and system integration. In the presented WDR imager design, much efforts have been done to reduce power dissipation by utilizing various design techniques at the circuit and logic level. These techniques have allowed reduction of both peak power dissipation (during the snapshot operation) and average power, dissipated by the pixel. The utilized methods can be divided into four main parts.

(a) Power reduction by leakage current control in analog and digital circuits – differentiation between the “active” and “sleep” modes of the certain circuit by insertion of a “sleep” transistor was applied on the in-pixel circuits like Mux and comparator. This technique relies on the reduction of the leakage current using the “stacked scheme” – by stacking two “off” transistors, the subthreshold leakage current is reduced significantly compared to a single off device due to simultaneous reductions in gate-source, body bias, drain-source voltages \[32\]. However, the insertion of sleep transistors slightly reduces the fill factor and increases the capacitance of the “Sleep” wire, which is shared by all pixels in the array and is driven by an external digital driver. Since the operation of the pixel is fully parallel, as described in Section II, the influence of the increase in the delay due to the insertion of the sleep transistors is negligible compared to the whole integration time (a few nano seconds compared to 30 milliseconds of the integration time).

(b) Low voltage operation – reduction of the power supply voltage is a key element in low-power CMOS imagers. However, the design of a low-voltage CMOS sensor involves several well-known challenges. Employing multiple voltage supplies can relax the problem. The idea of multiple \( V_{DD} \) grows up from the dual-\( V_{DD} \) approach in the digital circuit design, where the gates of the noncritical paths have the reduced supply voltage \( V_{DDL} \), while those on the critical paths have \( V_{DDH} \). This results in reducing the power without degrading the entire circuit performance. Similarly to the digital circuits, in the designed sensor high \( V_{DD} \) (1.8 V) was used in the critical places, significantly influenced by \( V_{DD} \) reduction, while low-voltage supply (1.2 V) was applied in others.

(c) Applying various low-power digital design styles for power reduction in the digital circuitry – in general, the custom design of the particular blocks in digital circuitry using nonstandard design techniques, like pass-transistor-logic (PTL) may significantly improve power dissipation. Custom digital design can be very useful when the in-pixel digital processing approach is used. In the presented WDR imager, a nonstandard low-power Mux, implemented using gate diffusion input (GDI) design technique was used. The GDI method is based on a simple cell that contains four terminals, allowing implementation of various complex functions using only
two transistors [33]. It has been proven that this Mux implementation leads to significant reduction in power dissipation, compared to a standard CMOS implementation. In addition, it employs only two transistors (M₀ and M₁₀) to implement the Mux functionality. In the case of the discussed snapshot pixel, a regular state of the Mux circuit is “Global Reset” = ‘1’ and “Comp Reset” = ‘1’ and if “Comp out” = ‘1’, therefore leakage current does not exist most of the time.

(d) Optimization of digital and analog sensor output chains – a standard three-transistor APS pixel includes only one analog output and two digital control inputs. An advanced sensor usually has more complicated structures. In addition to an increased number of analog outputs and digital control inputs, it can include digital outputs generated by the pixel. The demand for this increased number of pixel inputs and outputs, the desire for acceptable fill factor and the requirement for low-voltage operation result in the necessity to optimize the analog and digital sensor output chains for area efficient low-power low-voltage operation. In this design, the same output chain was employed both for analog and digital signals to reduce the area and power dissipation of the imager.

IV. EXPERIMENTAL RESULTS

A 32 × 32 imager was successfully fabricated using standard mixed-signal TSMC 0.35 μm process available through MOSIS. Each pixel has a size of 18 μm × 18 μm and a fill factor of 15%.

To verify the proposed concept, the fabricated test chip was tested using dual power supply voltages (1.2 and 1.8 V), as described in Section II. All control signals were generated externally using an field programmable gate array (FPGA) based test board. The output signals were downloaded to the PC, allowing image capture, processing and presentation. The test setup is shown in Fig. 4. The setup allowed imager operation at up to 1000 frames/s and DR extension of up to 8 bits.

Fig. 5 depicts an optical setup used for the test chip characterization. This setup is common for most of optical tests and consists of: a) a halogen lamp; b) a motorized filter wheel with a long-pass filters with cutoff wavelengths within the range of the visible light spectrum; c) monochromator; d) integrating sphere; and e) reference diode. The integration sphere is used to obtain a uniform illumination on the chip interface. Light intensity is controlled by the monochromator slit input and is measured by the reference photodiode.

The spectral response of the fabricated sensor is depicted in Fig. 6.

Fig. 7 shows measurements of the image sensor normalized output voltage as a function of incident illuminance without applying the WDR algorithm. The maximum quantum efficiency (QE) of 32% is achieved at 600 nm wavelength.
Fig. 8. Imager normalized output voltage as a function of incident illuminance: (a) without applying the WDR algorithm and (b) with 3 bits DR extension.

Each point represents an average of 50 frames for a given intensity. The sensor linearity and output swing is defined by the in-pixel source follower amplifier. Under these conditions, the measured DR is 49 dB. According to simulation results, presented in [30], the maximum DR without expansion was 57 dB. We assume that the main reasons of this discrepancy between the results are switched capacitor noise with sharing between the comparator and photodiode capacitor, kickback comparator noise, and reset path jitter that have not been taken in account in the analysis presented in Section III.

Fig. 8 presents comparison of the output voltage as a function of incident illumination measurements performed without applying the algorithm (similar to Fig. 8 and with 3 bits DR expansion (equivalent to 18 dB extension). It can be seen that the pixel performs reset operation each time the photodiode voltage reaches the comparator threshold according to the incident light intensity.

In this design, the comparator threshold ensures that the pixel will not saturate at the end of the integration time (see threshold voltage consideration in Section III). To do so, the output voltage in Fig. 8 does not reach its maximum possible value (630 mV) and is reset at 480 mV, reducing pixel SNR [22], [23].

Fig. 9, shows the scene observed by the proposed imager at different illumination conditions. The scene observed at room light illumination conditions is presented in (a). The same scene observed with a laser light on the object is shown in (b). In this test, the imager operated without WDR expansion. As can easily be seen, some of the pixels were saturated because of the strong light conditions. The scene observed at the same illumination conditions (with a strong light on the object) is seen in (c). However, in this case, 1-bit WDR expansion was applied. It can be clearly seen that, as expected, the part of the pixels saturated in (b), did not saturate in this case. Fig. 9(d) demonstrates the imager performance under the same illumination with 2 bits extension.

Note, both Fig. 9(c) and (d) aim to prove the functionality of the imager, showing only the Manual output of the imager. Therefore, the images give an impression of noise presence. In order to present the actual pixel values [see (1)], the value of each pixel has to be calculated according to (1) and should then be compressed to suit an 8-bit monitor resolution. There are many ways to present WDR imagers on 8-bit monitors [34], [35], however, this issue is out of scope for this paper.

Table I presents power dissipation of a single sensor for different illumination levels.

<table>
<thead>
<tr>
<th>WDR expansion</th>
<th>Dark</th>
<th>Room light (\Phi=4\times10^{12}) [ph/cm²sec]</th>
<th>Clear sky (\Phi=4\times10^{15}) [ph/cm²sec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(no expansion) ((\sim49\text{dB))}</td>
<td>21nW</td>
<td>22nW</td>
<td>23nW</td>
</tr>
<tr>
<td>4 bit expansion ((\sim73\text{dB))}</td>
<td>21nW</td>
<td>23nW</td>
<td>26nW</td>
</tr>
<tr>
<td>8 bit expansion ((\sim97\text{dB))}</td>
<td>21nW</td>
<td>23nW</td>
<td>29nW</td>
</tr>
</tbody>
</table>
whole array was measured and divided by 1024. The power was measured in three cases: (a) no DR expansion algorithm was applied; (b) expansion of 4 bit (equivalent to DR \(\sim 73\) dB); and (c) expansion of 8 bit (equivalent to DR \(\sim 97\) dB). As can be seen, the pixel has very low-power dissipation of 23 nW for 8 bit expansion at room light and 29 nW at high illumination level equivalent to clear sky. The power dissipation of the whole sensor (including the supporting circuitry) was 450 \(\mu\)W.

Since the proposed imager was implemented in 0.35 \(\mu\)m CMOS technology, a relatively large pixel size and a low fill factor have been achieved. The imager implementation in more advanced technologies can decrease the pixel size or/and increase the fill factor. Scaling to 0.18 \(\mu\)m and larger technologies is straightforward and can be easily calculated using a scaling factor. However, the scaling to more advanced processes (below 0.18 \(\mu\)m) is not straightforward since it may require techniques for more aggressive power reduction due to increased leakages. In addition, the reduced supply voltage in these technologies may also result in the need to change the in-pixel circuitry, while remaining with the same algorithm.

It is also very important to mention, that although a proof of concept for the small \(32 \times 32\) pixel array was presented, the array can be easily enlarged to any size since the pixels operation is fully parallel and the requirements for readout operation are relaxed. The only restriction on the array scaling to higher pixel counts is the peak power dissipation during the parallel operation of all pixels in the array. However, this issue can be resolved on the layout level by designing critical wires wide enough. It is obvious, that the size of the memory, decoders and S/H circuits will be scaled accordantly with the pixel array scaling.

Table II presents the chip attributes.

### Table II
**Image Sensor Performance Figures of Merit**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Size</td>
<td>32x32</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>18(\mu)m x 18(\mu)m</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35(\mu)m</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2 V and 1.8 V</td>
</tr>
<tr>
<td>Fill Factor</td>
<td>15%</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>32 (\mu)V/e</td>
</tr>
<tr>
<td>Dark Current Density</td>
<td>2.1 nA/cm(^2)</td>
</tr>
<tr>
<td>FPN</td>
<td>0.14%</td>
</tr>
<tr>
<td>Peak QE</td>
<td>32%</td>
</tr>
<tr>
<td>Inherent DR</td>
<td>49dB</td>
</tr>
<tr>
<td>Extended DR</td>
<td>Up to 97dB</td>
</tr>
<tr>
<td>Pixel power dissipation (max)</td>
<td>290nW @ 30fps</td>
</tr>
<tr>
<td>Imager power dissipation</td>
<td>450(\mu)W @ 30fps</td>
</tr>
</tbody>
</table>

V. CONCLUSION

We have presented a low-power global shutter CMOS image sensor with ultra-WDR. A prototype of \(32 \times 32\) pixels has been fabricated using the 1-poly 4-metal CMOS standard 0.35 \(\mu\)m process available through MOSIS and was successfully tested. The proposed imager performs snapshot image acquisition and offers a customized, linear, large increase in the dynamic range by implementing smart, low-power circuits for in-pixel auto-exposure. Driven by low-power dissipation requirements, the proposed pixel is operated by dual low voltage supplies (1.2 and 1.8 V) and utilizes an advanced low-power sensor design methodology. The measurements from the test chip have shown that the fabricated imager allows DR expansion of up to 97 dB.

### REFERENCES


Alexander Belenky received the B.Sc. degree in physics and the M.Sc. degree in electrophysics engineering from Ben Gurion University, Beer-Sheva, Israel, in 1995 and 2003, respectively. He is now working towards the Ph.D. degree at Ben Gurion University.

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M. D. Fairchild and G. M. Johnson, “iCAM framework for image ap-


Alexander Fish (S’04–M’06) received the B.Sc. degree in electrical engineering from the Technion, Israel Institute of Technology, Haifa, Israel, in 1999, and the M.Sc. degree in 2002 and the Ph.D. degree (summa cum laude) in 2006, respectively, from Ben Gurion University, Israel.

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Dr. Fish was honored with the Electrical Engineering Dean Award at Technion in 1997 and with the Technion President’s Award for Excellence in study in 1998, respectively. He was a co-author of two papers that won the Best Paper Finalist awards at the ICECS04 and ISCAS05 conferences. He was also awarded the Young Innovator Award for Outstanding Achievements in the field of Information Theories and Applications by ITHEA in 2005. In 2006, he was honored with the Engineering Faculty Dean “Teaching Excellence” recognition at Ben-Gurion University. He has served as a referee in the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, and Actuators Journal in the IEEE SENSORS JOURNAL, SPIE Optical Engineering Journal, as well as ISCAS, IEEE Sensors, and IEEE Sensors Conferences. He was also a co-organizer of several special sessions on “smart” CMOS Image Sensors at the IEEE Sensors Conference 2007 and on low-power “Smart” Image Sensors and Beyond at the IEEE ISCAS 2008.

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